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Full Length Research Paper

Fabrication of 6 nm gap on silicon substrate for power-saving appliances

T. S. Dhahi[1]*, U. Hashim[1], M. E. Ali[2] and N. M. Ahmed[3]

[1]Institute of Nano Electronic Engineering, Universiti Malaysia Perlis, 01000 Kangar, Malaysia.
[2]Nanotechnology and Catalysis Research Center, Universiti Malaya, 50603 Kuala Lumpur, Malaysia.
[3]School of Physics, Universiti Sains Malaysia, 11800 Penang, Malaysia.

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We document a thermal oxidation process for the reproducible fabrication of 6-nm gaps on silicon-on-insulator (SOI) substrate. Nanogaps sizes of this dimension are implicated to eliminate contributions from double-layer capacitance in the dielectric sensing of proteins or nucleic acids. The method combines conventional photolithography and pattern-size reduction technique to create a desired-size gap. The gaps are physically characterized with a field emission scanning electron microscopy (FESEM). Preliminary results show that gap-size reduction provides an improvement in conductivity, permittivity and capacitance parameters, reflecting the potential applications of the fabricated structures in low-power consuming electrical devices. The task is completed with two chrome masks: the first mask is for the nanogap pattern and the second one is for the electrodes. An improved resolution of pattern size is obtained by controlling the oxidation time of the final cycle. The reproducibility of the method is proven in triplicate experiments. We believe the method can be used in the industrial production of desired-size nanogaps on a variety of low-cost substrates.

Key words: Nanogap, sequential oxidation, wet etching, double-layer capacitance, dielectric sensing, biomolecules.

INTRODUCTION

The main objective of the study is to fabricate an electrode with a desired nanogap on low-cost substrates. The development of a cost-effective, easily performable and high-throughput technique for the fabrication of such structures is of great interests both for the possibility of increasing the device-packing density and reducing the power consumption (Namatsu et al., 2003). Such structures might have potential applications in the next generation nano-electronic devices, such as single electron transistors (Namatsu et al., 2003), metal/ insulator tunnel transistors (Sasajima et al., 1999), nanowire transistors (Marchi et al., 2006), nanotube- or nanoparticle-based devices (Allen and Kichambare, 2007; Ding et al., 2006). Chemical and biological nanosensors, biochips and nanobioelectronics are other areas of potential applications and are rapidly progressing (Schoning and Poghossian, 2006; Yogeswaren and Chen, 2008; Yih and Talpasanu, 2008, Poghossian et al., 2006). The coupling of biomolecules with nanomaterials (nanoparticles, nanotubes, etc) and nanostructures (e.g., nanoelectrodes, nanotransistors, nanogaps, nanopores, nanochannels) of comparable dimensions might allow the creation of hybrid systems with unique functions and applications (Tang et al., 2006; Zhang et al., 2008; Sigalov et al., 2008; Gun et al., 2008; Tsai et al., 2005; Liang and Chou, 2008; Cho et al., 2008). Such a functional hybrid systems, originated from the “marriage” of biomolecules and nano-scaled trans-ducers, provide a powerful tool, not only for manipulation and detection, but also for the fundamental research of single biological molecule (DNA, immunoglobulins, proteins, etc, and living cells).

The realization of different nanometer-sized structures has been demonstrated by advanced high-resolution nanolithography techniques, such as electron- or ion-beam lithography, focused ion-beam milling, scanning

*Corresponding author. E-mail: sthikra@yahoo.com.

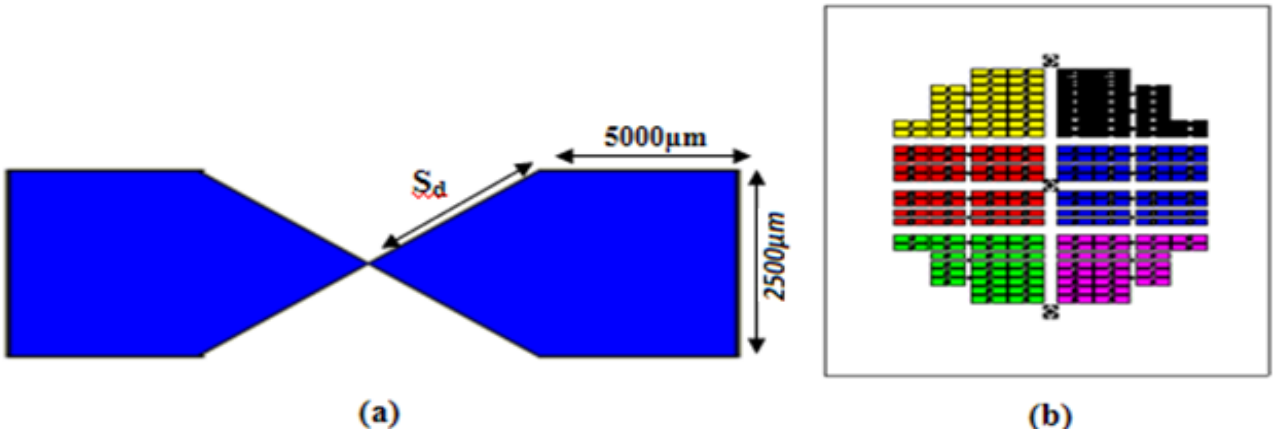


Figure 1. Schematic presentation of the first mask with dimension specification (a) and the actual mask on chrome glass (b).

tunneling or atomic force microscopy, nanoimprint lithography, and different top-down fabrication techniques (Chen and Pepin, 2001). Although these techniques provide high resolution in generating different nano-structures, most of them are time-consuming, low-throughput, complicated and expensive.

On the other hand, conventional photolithography is a low-cost technique with huge potentials. Recently, some non-conventional techniques in combination with conventional photolithography have been proposed for the preparation of nanoelectrodes, nanogaps and other nano-scaled devices. These techniques include, for instance, a photoresist thermal reflow and shrinking (Meng et al., 2001) or photoresist ashing technique (Kim et al., 2008), a shadow evaporation process (Ishida et al., 2005), a controlled size-reduction using the oxidation of Si (Choi et al., 2003; Hashioka et al., 2005; Cho et al., 2007) or laser-assisted electrochemical etching (Juhasz and Linnros, 2002), chemical–mechanical polishing (Lee et al., 2003), the decrease of separation between metallic electrodes by means of an electro-deposition from an electrolyte solution (Morpurgo et al., 1999), methods that utilize a sidewall structure (Chung et al., 2002), a self-aligned plasma etching of a silicon dioxide layer and silicon substrate (Georgiev et al., 2003), or a lateral, partial anodic oxidation of the side-edge of a photolitho-graphically-structured metallic film (e.g., Ti) (Hashioka et al., 2003), and techniques that use a silicon-on-insulator structure (Strobel et al., 2007).

An alternative solution for the fabrication of self-aligned nanostructures by means of conventional photolitho-graphy combined with pattern-size reduction techniques has recently been proposed (Platen et al., 2006; Poghossian et al., 2005). The method of the thermal oxidation is displayed by patterning nanostructures with different sizes and layouts on a silicon-insulator coated silicon material. The current report demonstrated the preparation of silicon nanogaps of less than 7 nm on a SiO_2–Si substrate. Less than 7 nm gap is expected to eliminate contributions from double-layer capacitance in the dielectric identification of protein, nucleic acid or small molecule (Di Carlo et al., 2003). A number of methods for fabricating nanogaps have already been established (Dhahi et al., 2010; Dhahi et al., 2011a, b, c, d, e, f). However, the reproducibility of those methods is not well proven. In the current research, we reproducibly fabricated 6 ± 2 nm gaps on silicon substrate with gold electrodes by the application of sequential thermal oxidation and buffer oxide etching (BOE). Preliminary results suggest such structure can be used in biomolecules sensing with a very low level of current supply.

MATERIALS AND METHODS

Mask design

A 100-mm p-type SOI ($Si_{Thickness}$ 1200 nm, SiO_2 = 150 ± 5 nm, Si = 15 µm) wafer is used as a substrate to fabricate the nanogap structure. We design two masks: one for the silicon nanogap (Figure 1) and the other (Figure 2) for the gold electrode by AutoCAD software. The masks are printed onto a chrome glass surface and purchased from a commercial company (Photonic Pte. Limited, Singapore). We apply dry etching (reactive ion etching (RIE)) to fabricate the gap and wet etching (buffer oxide etching (BOE)) to pattern the electrode structures. The anisotropy of RIE is modeled and the etching profiles are simulated elsewhere (Spelthahn et al., 2009).

Figure 1a shows the first mask for nanogap generation with a length of 5000 µm and a width of 2500 µm. The chrome mask with actual arrangement of the device design is shown in Figure 1b. It consists of 160 dies with 6 different layouts. The angle length of the end electrode is of 1/6th scale, starting from 100 to 1100 µm with an increment of 100 µm for each unit of S_d length.

This is simply for checking the best angle for the best nanogap formation after the etching process. The symbol S_d refers to the dimension of the side angle of the proposed nanogap. The sharpness of the nanogap proportionates to the dimension of S_d.

Figure 2a is a schematic device design of mask 2 with 1500 µm of length and 1500 µm of width. The distance between two rectangles is 3500 µm. The actual mask is shown on the chrome glass (Figure 2b).

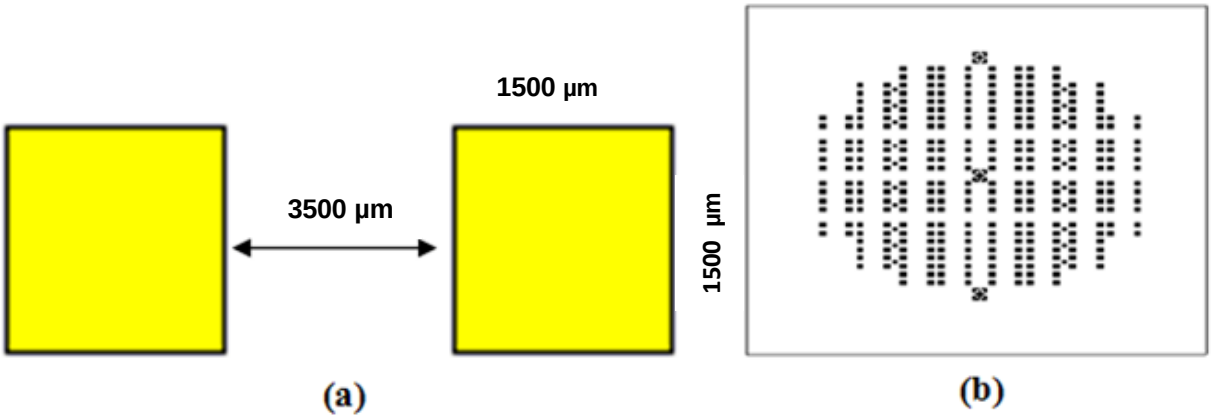


Figure 2. Design specification for mask 2 (a), and actual mask on chrome glass (b).

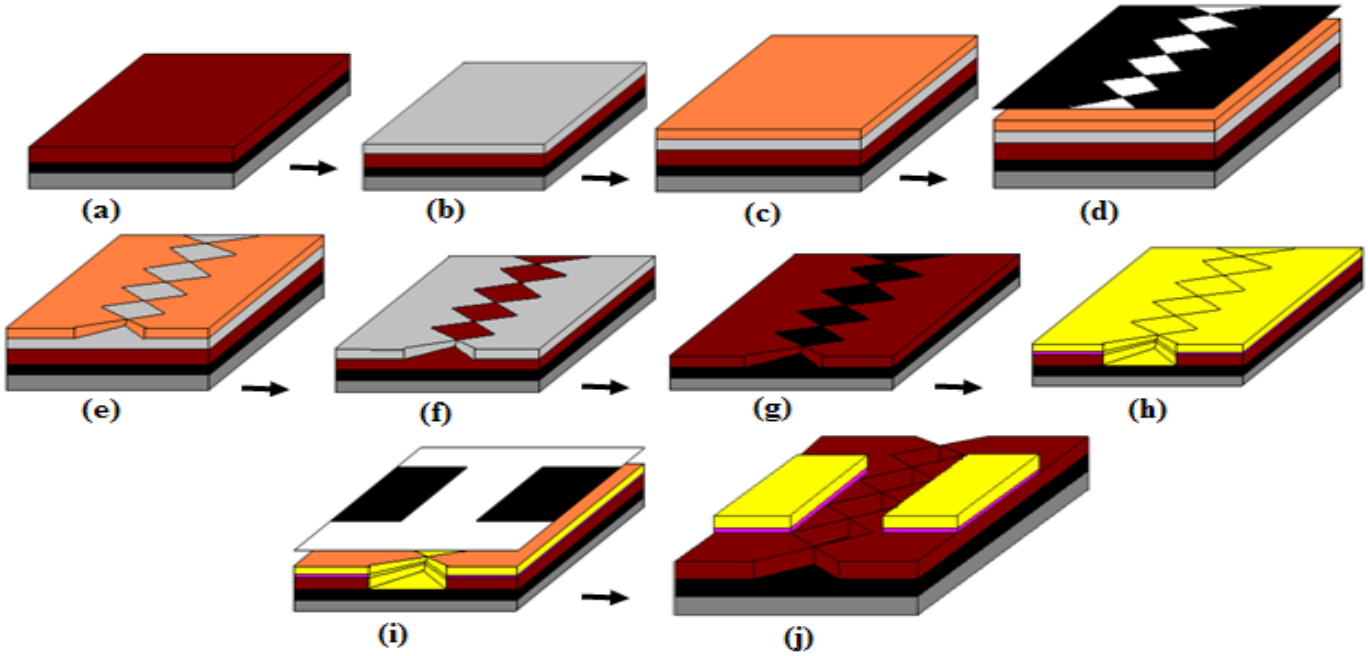


Figure 3. The process flow for the fabrication of nanogap on silicon substrate. Shown are: SOI wafer-starting material (a), a deposit of 135-nm Al-layer (b), a coating of photoresist (c), an exposure to Mask1 (d), a resist development (e), a wet etching of Al-layer (f), a dry etching of silicon layer (g), a deposit of Ti/Au-layer (h), an exposure to mask 2 (i) and final device after wet etching the Ti/Au-layer.

Fabrication of nanogap structure

The process flow for the fabrication of gold electrode with desired nanogap on SOI-wafer is shown in Figure 3. The process is started with the cleaning of the SOI wafer (a), followed by the deposition of 135-nm aluminum (Al) layer (b) as a hard mask by physical vapor deposition (PVD) instrument. This is to avoid damage to the silicon layer during the etching (RIE) process. The next step is the photolithography process. A layer of positive photoresist of 1200-nm thickness is applied on the aluminum substrate (c) and then exposed to ultraviolet light through Mask 1 (d). Following the development process (e), only the unexposed resist would remain. The wet-etching process of the aluminum layer (f) is performed before removing the resist. Subsequently, the dry etching process (g) for the silicon layer is done to fabricate the nanogap by reduction of gap size. A layer of 150 nm gold substrate is deposited over a 30 nm Ti-layer (h). In the following step, the resist coating is applied for resist development before exposing to Mask 2 (i). Finally, the wet-etching process of the Ti/Au substrate is performed to obtain the gold electrode with the silicon nanogap (j).

Before fabricating the electrode, the aluminum layer is wet-etched and silicon layer is dry etched, using a reactive ion etching (RIE) process, according to the mask layout. The structured silicon layer is oxidized at a temperature of 1000°C in dry O_2 atmosphere to form the oxide layer which is sequentially etched by BOE solution (Xiao, 2001). The oxidation time is varied from 10 to 20 min in each cycle of oxidation and etching, depending on the thickness of the silicon layer. The prepared structures are optically characterized

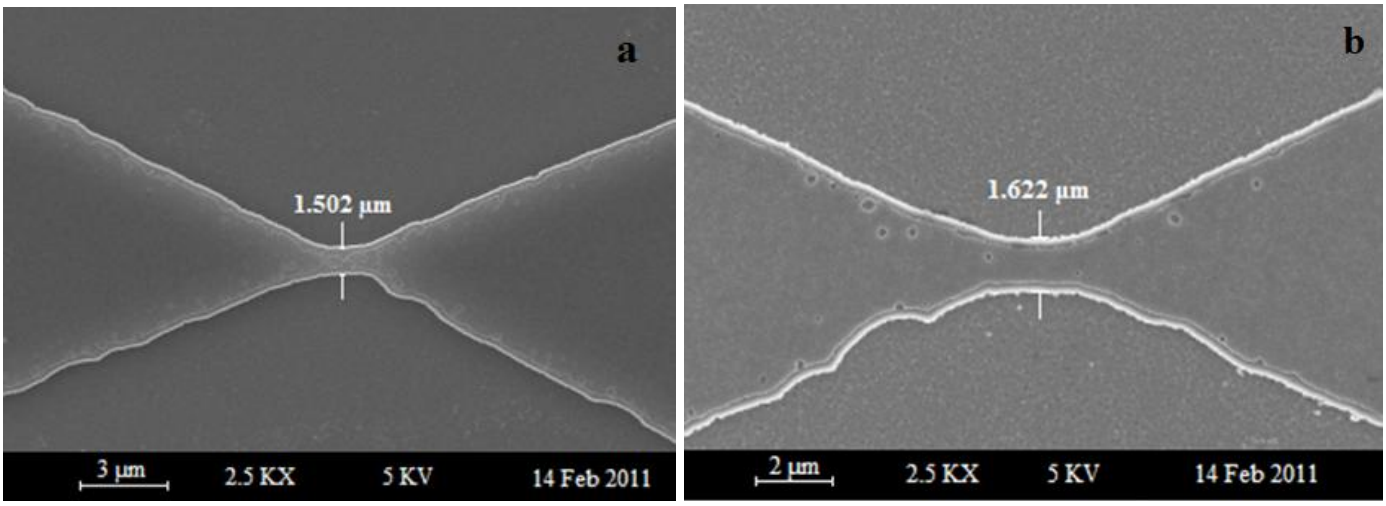


Figure 4. FESEM image of fabricated silicon pattern before (a) and after (b) thermal oxidation treatment and at the end of BOE (c).

with a FESEM (ZEISS FESEM ULTRA55) before and after the oxidation and etching processes of each cycle.

Electrical characterization

The final device with 89-, 33- and 6-nm of gaps is connected to a Dielectric Analyzer (Alpha-A High Performance Frequency Analyzer, Novocontrol Technologies, Handsangen, Germany) at room temperature to measure capacitance, permittivity and conductivity with air in the gap spaces.

RESULTS AND DISCUSSION

Nanogap fabrication

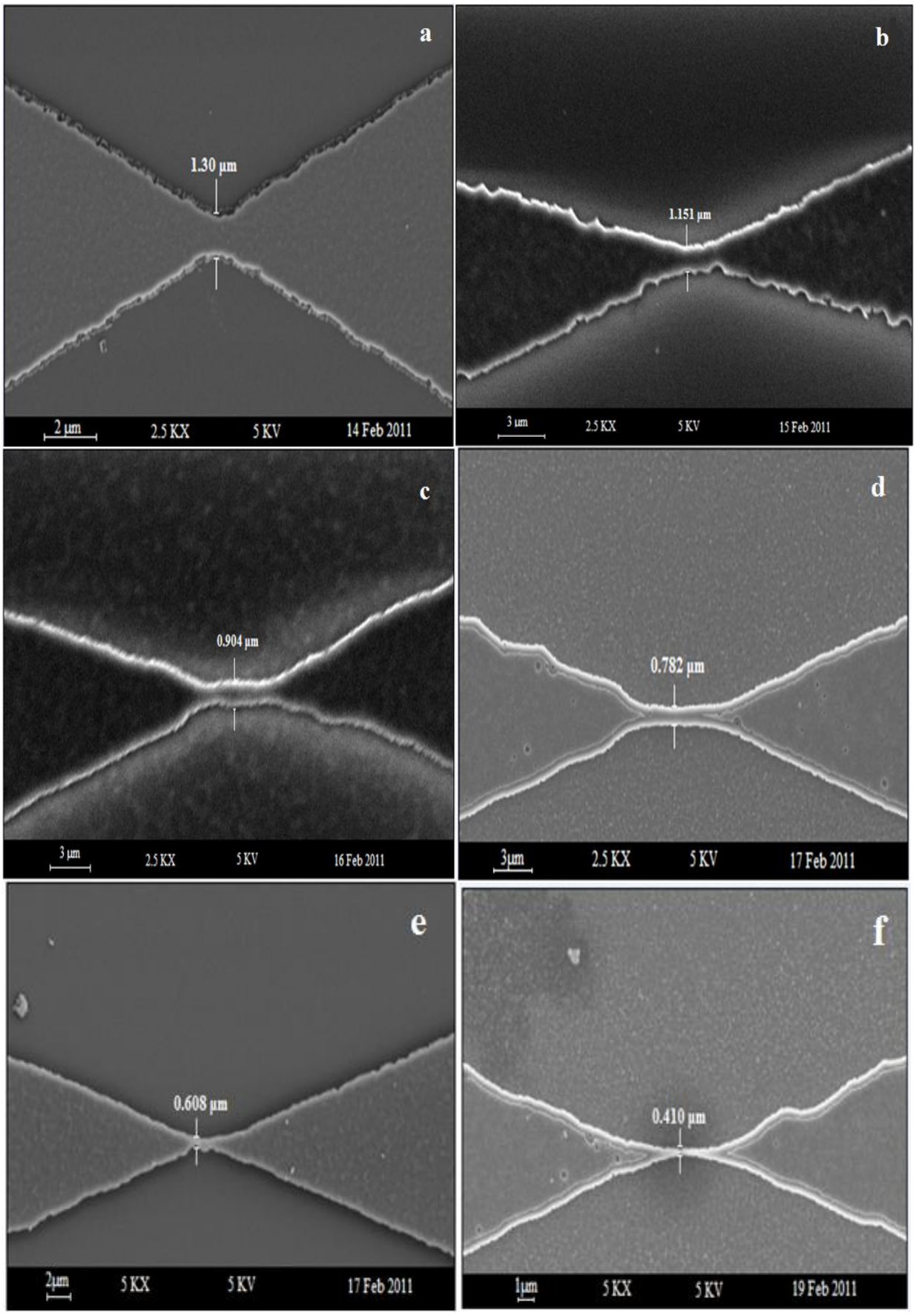
The FESEM cross-sectional images of an original photo lithographically-patterned silicon-layer before and after applying the oxidation process are shown in Figure 4. The thickness of the silicon layer plays an important role in the stability of the fabricated structure. According to our experience, fabricated structure are frequently broken down if a thin layer of silicon (<200 nm) is used. For the current experiment, a silicon layer of 1200 nm is chosen because of its higher stability in sequential thermal oxidation and etching. After patterning the silicon layer with the designed chrome mask, the width of the layer at gap location is 1.502 µm (shown by the gap width in Figure 4a). Then we apply sequential thermal oxidation and etching in alternate to create a nanogap at the desired position. An oxide layer of silicon dioxide (SiO_2) is created on silicon layer (Figure 4 b) by thermal oxidation at 1000°C for 20 min (Xiao, 2001) and then the fabricated oxide layer is stripped out completely (Figure 4c) by the etching process using buffer oxide etching (BOE) solution for 10 to 20 min (Rathi et al., 1995).

Figure 5 (a to i) shows the nanogap structure at the end of each cycle of oxidation and etching. We observe the silicon layer loses its width by 130 to 250 nm after each cycle of oxidation and etching, depending on the stages of cycles. Thus, at the end of the 9^{th} cycle, a 89 nm gap is realized (Figure 5i). We then reduce the oxidation time of the structure (Figure 5h) from 20 to 15 min. After etching with BOE solution for 10 to 20 min, a 33-nm gap is obtained (Figure 5j). Further reduction of the oxidation time to 10 min generates a 6-nm gap (Figure 5k). Repetition of the procedures in triplicate experiments generates a nanogap of diameter 6 ± 2 nm proving its reproducibility and feasibility to be used in batch production.

The precise control of nanostructure dimensions is a crucial point for a reproducible fabrication (Cosmin et al., 2010). The pattern size reduction technique can generate an excellent reproducibility by controlling the thickness of oxide layer (Xiao, 2001). Thus, the size of the nanogap structure can be precisely controlled by careful selection of oxidation time. In order to see the effect of oxidation time on the pattern-size reduction of the silicon layer, the 9^{th} cycle oxidation time and the corresponding thickness of the oxide layer along with the size of the fabricated gap are measured. A plot of oxide layer thickness and oxidation time (Figure 6a) demonstrates a proportional relationship with very good linearity (R^2 = 0.991). Linear relationship (R^2 = 0.958) is also observed between nanogap-size and oxidation time when they are plotted in a graph (Figure 6b). A plot of nanogap-size versus oxide-layer thickness reveals gap-size which proportionate over the time of oxidation (R^2 = 0.978) (Figure 6c).

Electrical properties of fabricated nanogap electrodes

Electrical sensing of biomolecules (proteins and nucleic


a
1.30 µm
2 µm
2.5 KX
5 KV
14 Feb 2011
b
1.151 µm
3 µm
2.5 KX
5 KV
15 Feb 2011
c
0.904 µm
3 µm
2.5 KX
5 KV
16 Feb 2011
d
0.782 µm
3µm
2.5 KX
5 KV
17 Feb 2011
e
0.608 µm
2µm
5 KX
5 KV
17 Feb 2011
f
0.410 µm
1µm
5 KX
5 KV
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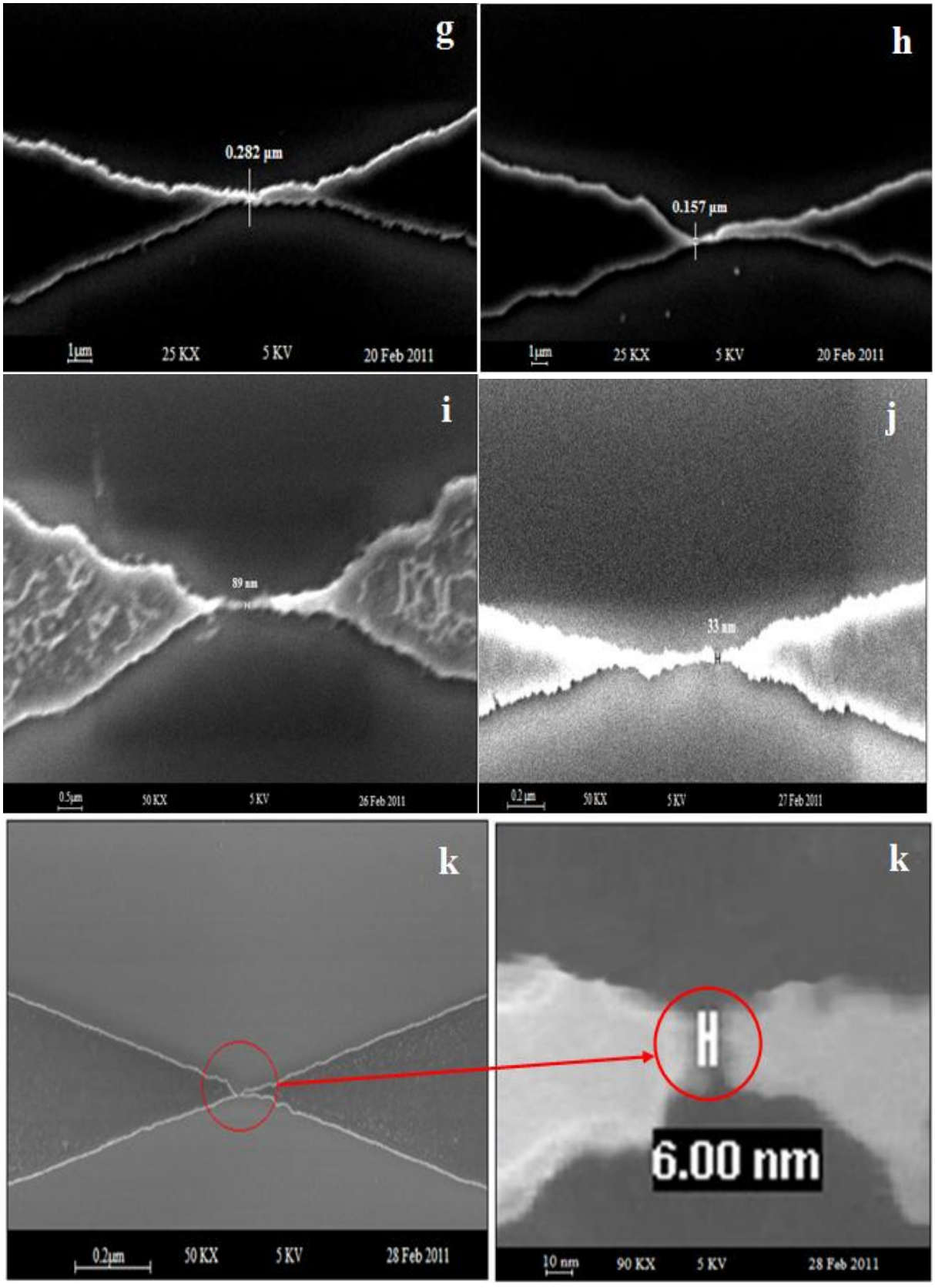

Figure 5. The FESEM images of the nanogap structure after etching with BOE solution at the end of each thermal oxidation step. Shown are the silicon layers after BOE etching at the end of the 1st to the 9th cycles with 20 min of oxidation (a to i) and the 9th cycle with 15 min (j) and 10 min (k) of thermal oxidation.

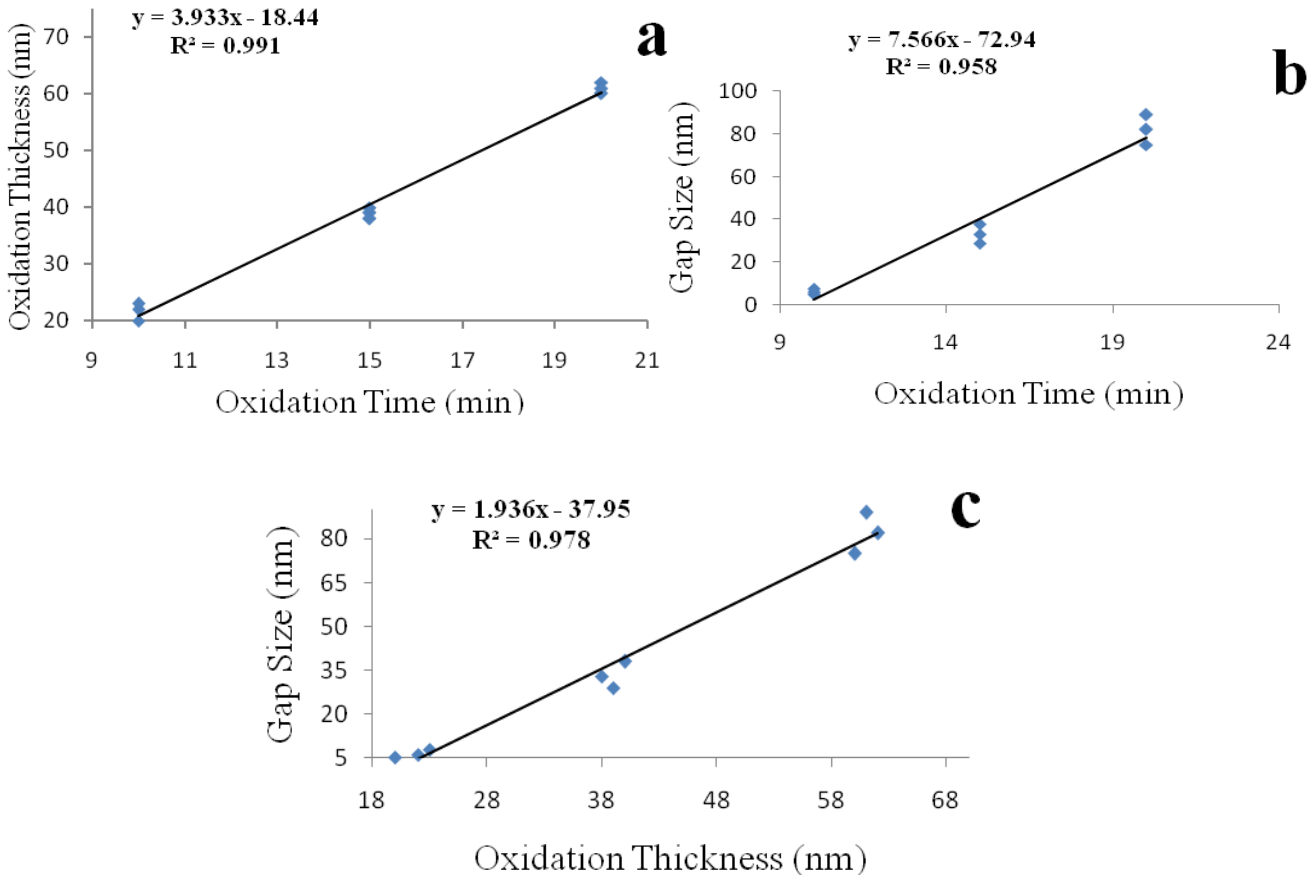

Figure 6. The thickness of oxide layer (a) and gap-size (b) as a function of the 9th cycle oxidation time. The relationship of gap-size and oxidation-thickness is shown in (c).

acids) solely relies on the measurement of current and/or voltage to identify target binding (Drummond et al., 2003). Usually a probe biomolecule is immobilized in the nanogap between the electrode pair and electrical properties are measured to come up with a decision whether the detection is achieved or not (Xing et al., 2010). Detection with low voltage or current is desired as high voltage may burn the anchored biomolecule probes and targets simultaneously, causing the device failure in biological sensing (Sang et al., 2009). Gap-size reduction should allow the electrode-structure to detect target biomolecule binding with very low supply of current.

Figure 7 (a to c) shows the capacitance and permittivity and conductivity profiles of 89-, 33- and 6-nm gap electrodes fabricated in the current experiment. The results clearly reflect increment of all three parameters with the reduction of gap-size. This can be explained with following simple equation that explains the operating principle of a capacitor:

$$C=\acute{\varepsilon}*A/d \quad (1)$$

where: $\acute{\varepsilon} = \varepsilon/\varepsilon^{o}$; $\acute{\varepsilon}$: the permittivity; ε^{o}: the permittivity for air in the free space; C: the capacitance value; A: the surface area of the nanogap structure, and d: the size of the gap/distance between the two plates.

Since the gap-size (d) is the denominator of the preceding equation, reduction of gap-size should increased capacitance of a nanogap capacitor (Mingqiang et al., 2004). The equation also reflects that permittivity and capacitance have a linear relationship. Therefore, permittivity enhancement by gap-size reduction is a logical outcome.

Permittivity reflects the index of a material's ability to transmit current without imposing a resistance (Ala'eddin and Poopalan, 2011). On the other hand, conductivity is a measure of a substance capacity to allow the passage of current. Thus the relation of permittivity and conductivity is proportional. Therefore, an increment of capacitance, permittivity and conductivity (Figure 7) with gap-size reduction suggests the fabricated nanogap structure can be used in bio-sensing applications with the minimum supply of power.

Nanogap structures are also implicated to eliminate the formation of electrical double layer between the electrodes in dielectric sensing of proteins and nucleic acids

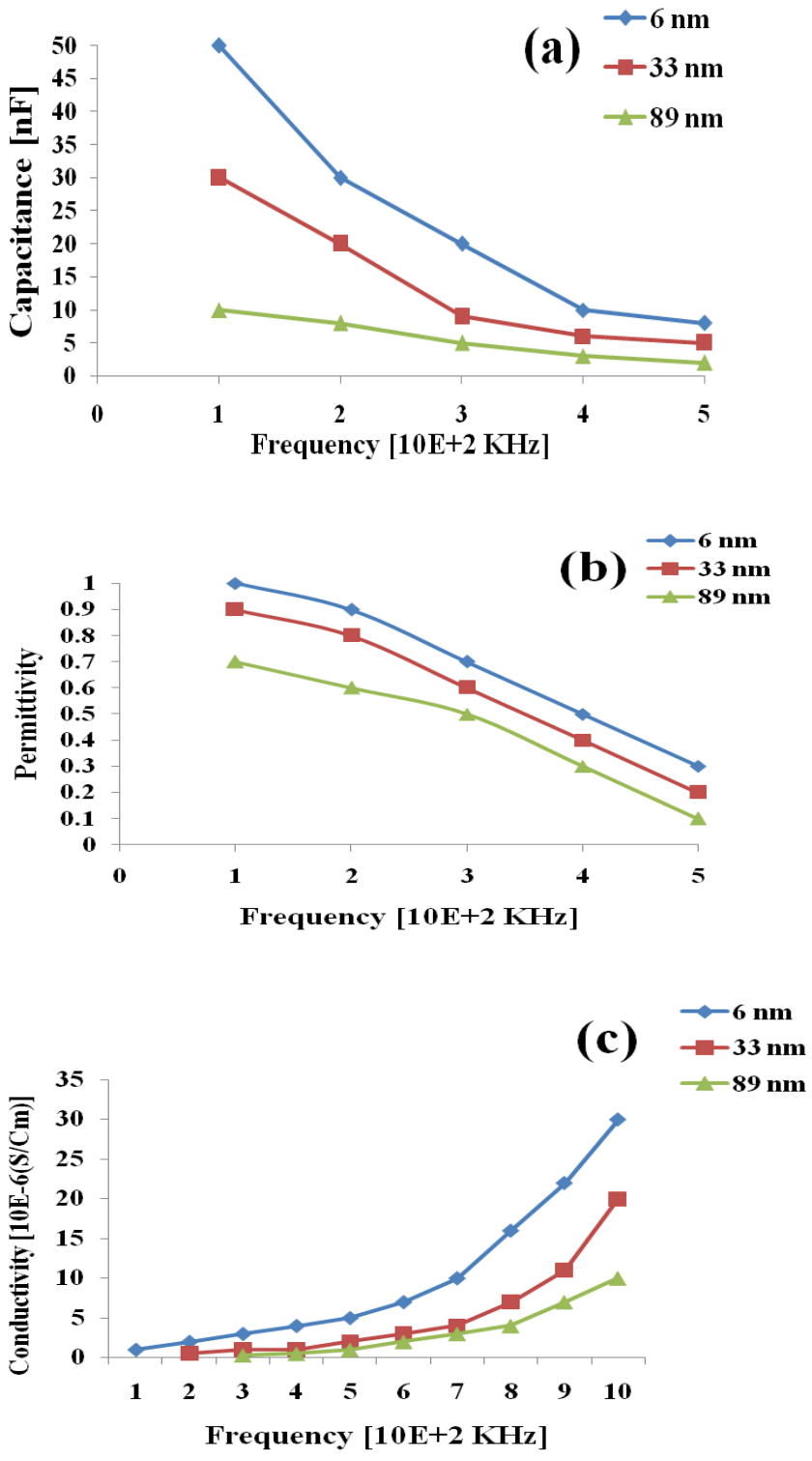

Figure 7. Capacitance, permittivity and conductivity profiles of different nanogap electrodes: (a) 6 nm; (b) 33 nm; and (c) 89 nm.

(Di Carlo et al., 2003). Dielectric detection of biomolecules is interesting as it is label-free and does not need any reference electrode (Berggren and Johansson, 1997). In the current experiment, no dielectric measurement is performed as it can be done only after immobilizing the probe biomolecule in the appropriate

nanogap. However, our group is working to do it in near future and will be reported in a separate publication.

Limitation and efficacy of the current method

The current method of fabricating nanogap etches up the surfaces of the plates that separated the gap to some extent. More benefit of the desired properties can be realized if integrity of the silicon layer can be restored. However, measurement of capacitance, permittivity and conductivity clearly reflects certain advantages of the 6-nm gap structure over those of 33 and 89-nms showing its feasible application in low-current consuming electrical devices. Moreover, the potential of the current method in reproducible fabrication of the desired nanogap has made it a suitable candidate in batch production.

Conclusion

A simple method for the fabrication of 6 nm gap using silicon material on a Si–SiO_2 substrate is developed. The method combines the conventional lithography and pattern-size reduction techniques to fabricate desired nanogap in a reproducible manner which is essential in batch production. Measurement of several electrical parameters strongly suggests that the structure can be used in electrical devices that consume very low-level of electricity. The fabricated structure should be able to detect biomolecules with the minimal supply of electrical current.

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