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Full Length Research Paper

Modeling and simulation of UPFC using PSCAD/EMTDC

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This paper proposes to model and simulate a unified power flow controller (UPFC) in power system computer aided design and electromagnetic transient direct current (PSCAD/EMTDC) environment. The series converter of the UPFC controls the transmission line real/reactive power flow and the shunt converter of the UPFC controls the UPFC bus voltage/shunt reactive power and the DC link capacitor voltage. The real power demand of the series converter is supplied by the shunt converter of the UPFC via the DC link capacitor. The control of transmission line reactive power flow leads to excessive voltage excursion of the UPFC bus voltage. In this proposed work, we have considered two system cases. The first case is to cause a sudden increase in the system load. The second case is to introduce a transient fault in the system. In both cases, excessive bus voltage excursions occur. A UPFC is modeled and designed to reduce these bus voltage excursions, and also proper coordination between the series and shunt converter controllers of the UPFC is maintained to limit the collapse of DC capacitor voltage. PSCAD/EMTDC software is utilized to design and simulate the model.

Key words: Unified power flow controller (UPFC), coordinated control, proportional integral (PI), power system computer aided design and electromagnetic transient direct current (PSCAD/EMTDC).

INTRODUCTION

The technology of power system utilities around the world has rapidly evolved with considerable changes in the technology along with improvements in power system structures and operation. The ongoing expansions and growth in the technology, demand more optimal and profitable operation of a power system. In the present scenario, most of the power systems in the developing countries with large interconnected networks share the generation reserves to increase the reliability of the power system. However, the increasing complexities of large interconnected networks had fluctuations in reliability of power supply, which resulted in system instability, difficult to control the power flow and security problems that resulted large number blackouts in different parts of the world. The reasons behind the stated fault sequences may be due to the systematical errors in planning and operation, weak interconnection of the power system, lack of maintenance or due to overload of the network. In order to overcome these consequences and to provide the desired power flow along with system stability and reliability, installations of new transmission lines are required. However, installation of new transmission lines with the large interconnected power system are limited to some of the factors like economic cost, environment related issues. These complexities in installing new transmission lines in a power system challenges the power engineers to research on the ways to increase the power flow with the existing transmission line without reduction in system stability and security (Hingorani and Gyugyi, 2000; Mohan Mathur and Rajiv, 2002; Acha et al., 2002).

Gyugyi (1992) proposed the unified power flow controller (UPFC). It is the most versatile and complex power electronic device introduced to control the power flow and voltage in the power systems. It is designed by combining the features of FACTS controllers - static synchronous series compensator (SSSC) and static synchronous compensator (STATCOM). It has the ability to control active and reactive power flow of a transmission line simultaneously in addition to controlling

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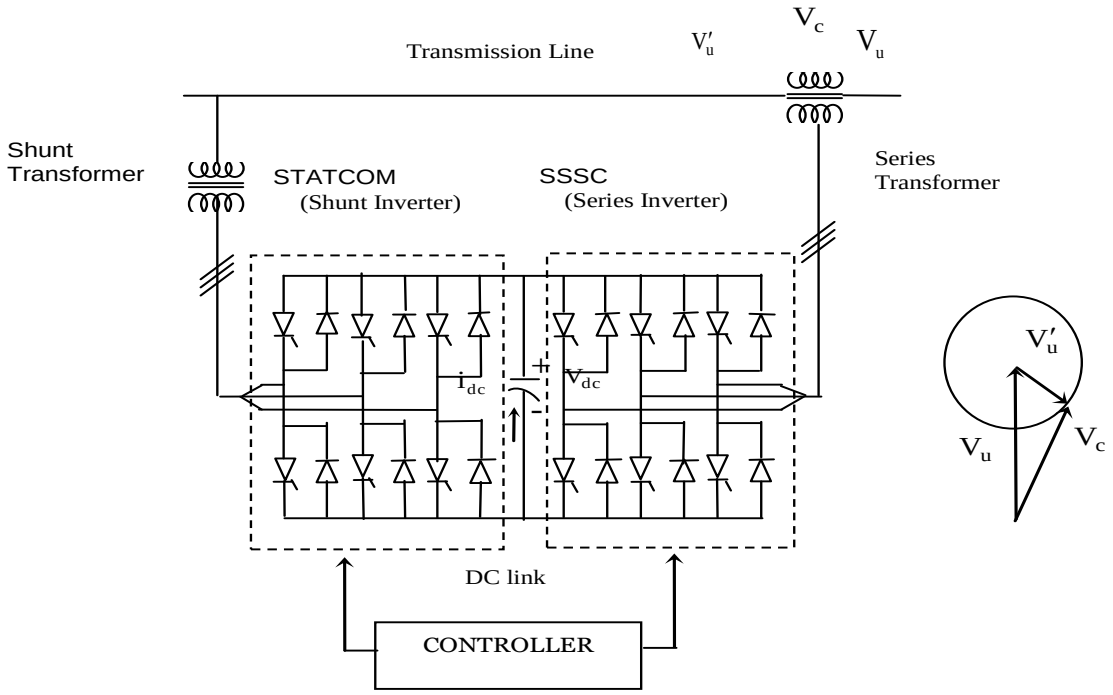

Figure 1. Basic circuit configuration of the UPFC.

all the transmission parameters (voltage, impedance and phase angle) affecting the power flow in a transmission line. The basic control for the UPFC is such that the series converter of the UPFC controls the transmission line real or reactive power flow and the shunt converter of the UPFC controls the UPFC bus voltage/shunt reactive power and the DC link capacitor voltage.

Several articles are reported on UPFC for different studies, namely improvement in transient stability and damping of rotor swing. Padiyar and Kulkurni (1998) proposed a control strategy for the UPFC for real power flow control by reactive voltage injection and indirect reactive power flow control by control of voltage at the two ports of the UPFC. The controllers are designed independently and use locally available measurement. Krishna and Padiyar (2005) proposed a method that involves the solution of a constrained optimization problem to determine the voltage and current injected by the UPFC, so as to maximize or minimize the power flow in the line in which it is located at each step. Kannan et al. (2004) proposed a cascaded proportional integral (PI) controller design to limit excessive voltage excursions during reactive power transfers.

In steady state, the real power demand of the series converter is supplied by the shunt converter of the UPFC. To avoid instability/loss of DC link capacitor voltage during transient conditions, a real power coordination controller was designed. Also, the need for reactive power coordination controller for UPFC arises from the fact that excessive bus voltage (the bus to which the shunt converter is connected) excursions occur during reactive power transfers. Here, the UPFC is modeled and designed to reduce these bus voltage excursions and also proper coordination between the series and shunt converter controllers of the UPFC is maintained to limit the collapse of DC capacitor voltage. The simulation results for a case study indicate that this is a viable control scheme, while this paper gives basic strategy and design consideration, further refinement is possible in the context of the recent advances in control strategy.

In this paper, first, the modeling of synchronous generator along with automatic voltage regulator (AVR), power system stabilizer (PSS) and modeling of UPFC were derived. Subsequently, the coordinated control schemes of UPFC were designed in PSCAD/EMTDC environment (Introduction to PSCAD/EMTDC, 2000) and simulation results are discussed under different loading and transient disturbance condition.

BASIC CIRCUIT CONFIGURATION OF UPFC

The principal function of the UPFC is to control the flow of real and reactive power by injecting a voltage in series with the transmission line. The UPFC consists of two solid-state voltage source inverters (VSIs) connected by a common DC link that includes a storage capacitor shown in Figure 1.

The first inverter (shunt inverter) known as a STATCOM injects an almost sinusoidal current of variable magnitude at the point of connection. The second inverter (series inverter), known as SSSC provides the main functionality

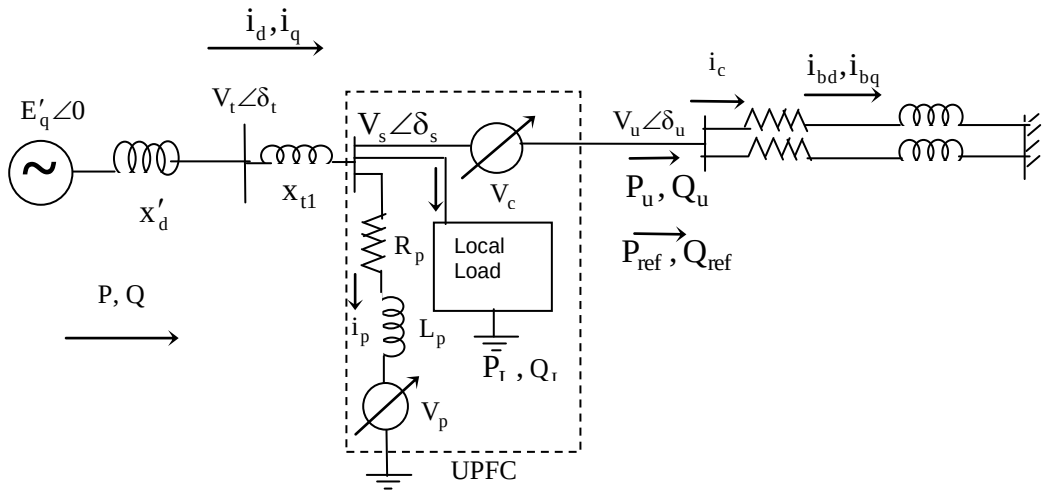

Figure 2. One-line circuit diagram model of UPFC installed in a power system.

of the UPFC by injecting an alternating current (AC) voltage V_c, with a controllable magnitude ($0 \le V_c \le V_c^{max}$) and phase angle ($\ge 0°$, $\le 360°$). Thus, the complete configuration operates as an ideal AC to AC power converter in which real power can flow freely in either direction between the AC terminals of the two inverters. The phasor diagram in Figure 1 shows that the UPFC is able to inject a controlled series voltage V_c into the transmission line. Thus, the magnitude and angle between the sending and receiving end of the transmission line are modulated resulting in power flow control in the transmission line. Therefore, the active power controller can significantly affect the level of reactive power flow and vice versa. In order to improve the dynamic performance and reduce the interaction between the active and reactive power control, the watt-var decoupled control algorithm was proposed. In addition, each inverter can independently modulate reactive power at its own AC output terminal (Sharma and Jagtap, 2010).

MATHEMATICAL MODEL OF UPFC

Single machine infinite bus power system is considered in this work. The mathematical models for the system components along with their control systems are described as follows:

Synchronous generator modeling

The synchronous generator is described by a third-order nonlinear mathematical model given by Equations 1 to 3.

$$\frac{d\delta}{dt} = \Delta\omega \tag{1}$$

$$\frac{d\Delta\omega}{dt} = \frac{1}{M}\left[P_m - E'_q i_q - \left(x_q - x'_d\right) i_d i_q\right] \tag{2}$$

$$\frac{dE'_q}{dt} = \frac{1}{T'_{do}}\left[E_{fd} - E'_q - \left(x_d - x'_d\right) i_d\right] \tag{3}$$

Where $\Delta\delta = \delta - \delta_0$ and $\Delta\omega = \omega - \omega_0$.

Dynamical modeling of UPFC

Figure 2 shows the equivalent circuit model of a power system equipped with a UPFC. The series and shunt VSIs are represented by controllable voltage sources V_c and V_p, respectively. R_p and L_p represent the resistance and leakage reactance of the shunt transformer.

The dynamic model of UPFC is derived by performing standard d-q transformation of the current through the shunt transformer and series transformer and is presented in Equations 4 to 7.

Shunt inverter

$$\frac{di_{pd}}{dt} = -\frac{R_p}{L_p} i_{pd} + \omega i_{pq} + \frac{1}{L_p}(V_{sd} - V_{pd}) \tag{4}$$

$$\frac{di_{pq}}{dt} = -\frac{R_p}{L_p} i_{pq} - \omega i_{pd} + \frac{1}{L_p}(V_{sq} - V_{pq}) \tag{5}$$

Series inverter

$$\frac{di_{bd}}{dt} = -\frac{w_b r_e}{x_e} i_{bd} + \omega i_{bq} + \frac{w_b}{x_e}(V_{ud} - V_b \sin\delta) \quad (6)$$

$$\frac{di_{bq}}{dt} = \frac{w_b r_e}{x_e} i_{bq} - \omega i_{bd} + \frac{w_b}{x_e}(V_{uq} - V_b \cos\delta) \quad (7)$$

Where ω is the angular frequency of the voltages and currents.

For fast voltage control, the net input power should instantaneously meet the charging rate of the capacitor energy. Thus, by applying power balance conditions, we get Equation 8.

$$P_s - P_u = V_{sd}(i_{pd} + i_{bd}) + V_{sq}(i_{pq} + i_{bq}) - (V_{ud} i_{bd} + V_{uq} i_{bq})$$

$$= V_{dc}\, i_{dc}$$

$$= V_{dc}\left[C\frac{dV_{dc}}{dt} + g_{cp} V_{dc} \right] \quad (8)$$

Thus, Equation 8 can be rearranged and written as given in Equation 9.

$$\frac{dV_{dc}}{dt} = -\frac{g_{cp}\omega}{b_{cp}} V_{dc} + \frac{1}{CV_{dc}}\left[\begin{array}{l} V_{sd} i_{pd} + V_{sq} i_{pq} + \\ (V_{sd} - V_{ud}) i_{bd} + (V_{sq} - V_{uq}) i_{bq} \end{array} \right] \quad (9)$$

COORDINATED CONTROL STRATEGY FOR UPFC

Proper coordination between the series and shunt converter control system in the UPFC has to be established. If proper coordination is not established, it could lead to collapse of the DC link capacitor voltage. The voltage level of the DC link capacitor is maintained by the shunt converter. Real power demanded by the series converter is also supplied by the shunt converter via the DC link capacitor. During sudden changes in the system such as system load or transient faults, there will be reduction in the bus voltages. Regulation of the bus voltages can be done by appropriate reactive power transfers. During such reactive power transfers, proper coordination has to be maintained in the UPFC to avoid collapse of DC link capacitor voltage. Thus, proper coordination of real and reactive power in the UPFC has to be maintained. In this paper, a simultaneous control of the UPFC controllers is done to enable appropriate coordination in the UPFC thereby enabling bus voltage regulation and avoidance of DC capacitor voltage collapse. Therefore, in the PI control scheme, the control strategies for both the inverters are addressed separately. The modeling and control design are carried out in the standard synchronous d-q frame (Juan et al., 2005).

Series inverter control

An appropriate series voltage (both magnitude and phase) should be injected for obtaining the commanded active and reactive power flow in the transmission line, that is, (P_u, Q_u). The current references are computed from the desired power references and are given by Equations 10 and 11.

$$i_{cd}^{ref} = \frac{P_{ref} V_{ud} - Q_{ref} V_{uq}}{V_u^2} \quad (10)$$

$$i_{cq}^{ref} = \frac{P_{ref} V_{uq} - Q_{ref} V_{ud}}{V_u^2} \quad (11)$$

The power flow control is then realized by using appropriately designed controllers to force the line currents to track their respective reference values. Conventionally, two separate PI controllers are used for this purpose. These controllers output the amount of series injected voltages (V_{cd}, V_{cq}).

Shunt inverter control

As mentioned earlier, the conventional control strategy for this inverter concerns with the control of AC-bus and DC-link voltage. The dual control objectives are met by generating appropriate current reference (for $d-$ and $q-$axis) and then, by regulating those currents. PI controllers are conventionally employed for both the tasks, while attempting to decouple the $d-$ and $q-$axis current regulators.

The inverter current (i_p) is split into real (in phase with ac-bus voltage) and reactive components. The reference value for the real current is decided so that the capacitor voltage is regulated by power balance. The reference for reactive component is determined by AC-bus voltage regulator. As per the strategy, the original currents in d-q frame (i_{pd}, i_{pq}) are now transformed into another frame, $d'-q'$ frame, where $d'-$ axis coincides with the ac-bus voltage (Vs), as shown in Figure 3. Thus, in $d'-q'$ frame, the currents $i_{pd'}$ and $i_{pq'}$ represent the real and reactive currents and are given by Equations 12 and 13.

$$i_{pd'} = i_{pd}\cos\delta_s + i_{pq}\sin\delta_s \quad (12)$$

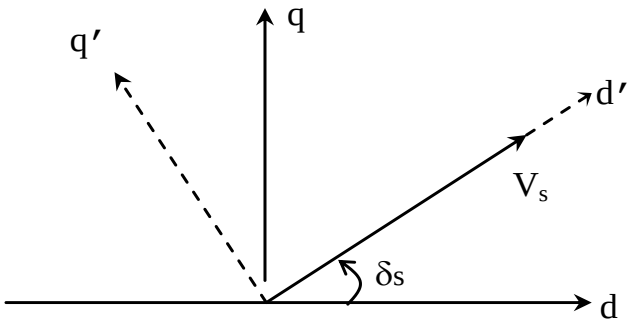

Figure 3. Phasor diagram showing d-q and d′-q′ frame.

$$i_{pq'} = i_{pq}\cos\delta_s - i_{pq}\sin\delta_s \quad (13)$$

Now, for current control, the same procedure has been adopted by re-expressing the differential equations as given in Equations 14 to 18.

$$\frac{di_{pd'}}{dt} = -\frac{R_p}{L_p} i_{pd'} + \omega i_{pq'} + \frac{1}{L_p}(V_s - V_{pd'}) \quad (14)$$

$$\frac{di_{pq'}}{dt} = -\omega i_{pd'} - \frac{R_p}{L_p} i_{pq'} + \frac{1}{L_p}(-V_{pq'}) \quad (15)$$

where

$$V_{pd'} = V_{pd}\cos\delta s + V_{pq}\sin\delta s \quad (16)$$

$$V_{pq'} = V_{pq}\cos\delta_s - V_{pd}\sin\delta s \quad (17)$$

and

$$\omega = \omega_0 + \frac{d\delta_s}{dt} \quad (18)$$

The VSI voltages are controlled as given in Equations 19 and 20.

$$V_{pq'} = -(\omega L_p i_{pd'} + L_p u_{q'}) \quad (19)$$

$$V_{pd'} = \omega L_p i_{pq'} + V_s - L_p u_{d'} \quad (20)$$

By substituting the above expressions for $V_{pd'}$ and $V_{pq'}$ in Equations 14 and 15, the following sets of decoupled equations are obtained.

$$\frac{di_{pd'}}{dt} = -\frac{R_p}{L_p} i_{pd'} + u_{d'} \quad (21)$$

$$\frac{di_{pq'}}{dt} = -\frac{R_p}{L_p} i_{pq'} + u_{q'} \quad (22)$$

Conventionally, the control signals $u_{d'}$ and $u_{q'}$ are determined by linear PI controllers.

In this study, the stated design was used for demonstration of UPFC control scheme. This approach led to good control as illustrated by the simulation results shown in later section.

CIRCUIT DESCRIPTION AND PROBLEM STATEMENT

In order to illustrate the design and implementation of the UPFC, a single phase circuit where the UPFC is connected between the source and the load is selected as shown in Figure 4. It consists of a 3-phase source connected to Bus1. Loads 1 and 2 are connected to Bus 2. There are two transmission lines connecting Buses 1 and 2. The shunt converter of the UPFC is connected to Bus 1 through a shunt coupling transformer. The series converter of the UPFC is connected to transmission Line 2 through a series coupling transformer. Controllers are designed to co-ordinate real and reactive power transfer in the UPFC and thereby to efficiently operate the UPFC. Load 1 is permanently connected to the system Bus 2. Load 2 is connected to Bus 2 only at a specific time interval. Due to the sudden increase in the system load, there is a drop in the bus voltages. Also, a transient 3-phase fault is introduced into the system at a specific time. Due to the sudden transient fault, there is a drop in the bus voltages. UPFC should be operated in such a manner to compensate the drop in the bus voltage by generating the required amount of reactive power and supplying it to its connected bus. Also, the collapse of the DC capacitor voltage has to be avoided. The electromagnetic transient modeling of UPFC for the test case study using PSCAD/EMTDC is shown in Figure 5.

CONTROLLER CIRCUIT

The controller circuit provides detailed description regarding the generation of firing pulses for both shunt and series converter under various operating conditions. The methodology by which proper co-ordination is maintained between the shunt and series converter is also discussed. The associated control schemes are shown in Figures 6 and 7.

Shunt converter controller

Shunt converter controller circuit describes the technique by which the angle order is generated based on changes in parameters of the main circuit. Utilizing this angle, the

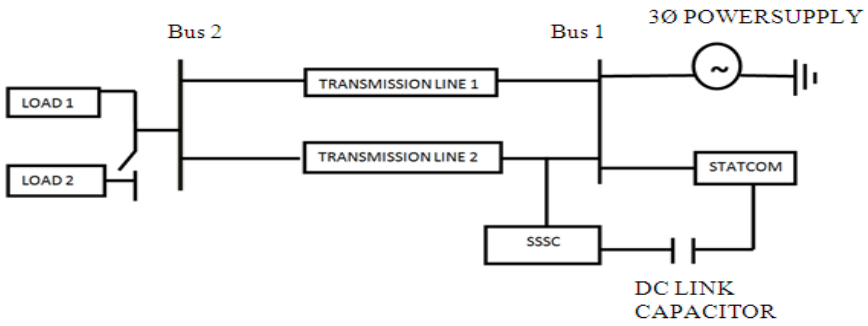

Figure 4. Basic block diagram of the circuit

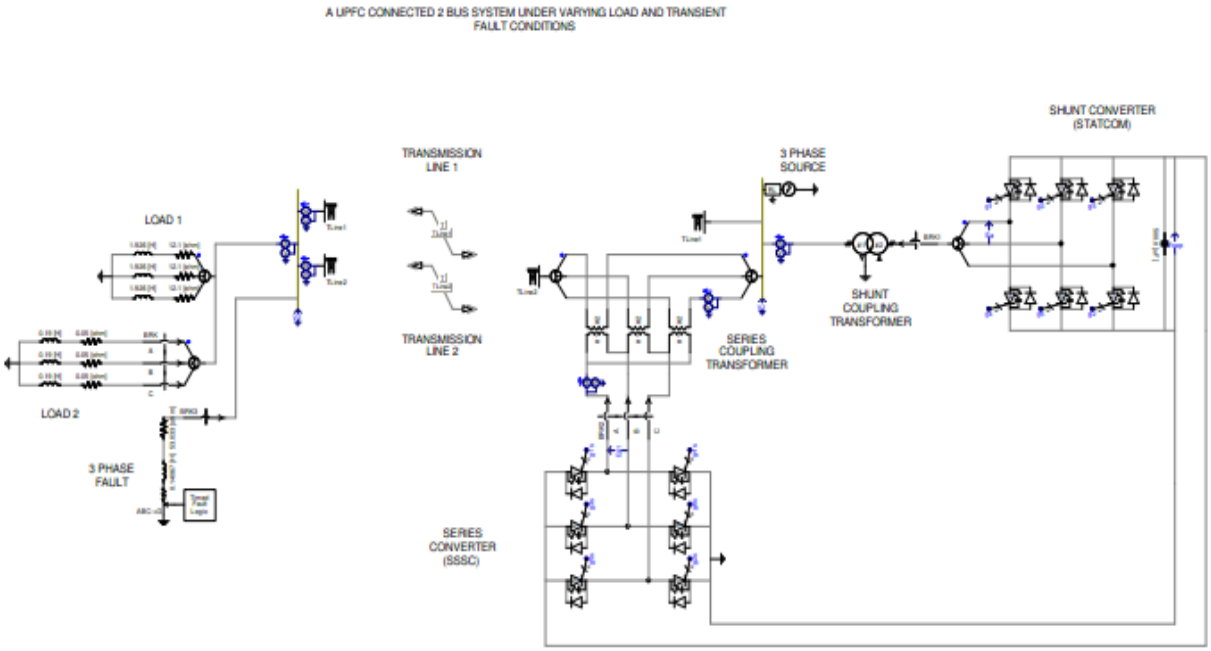

Figure 5. Electromagnetic transient modeling using PSCAD/EMTDC.

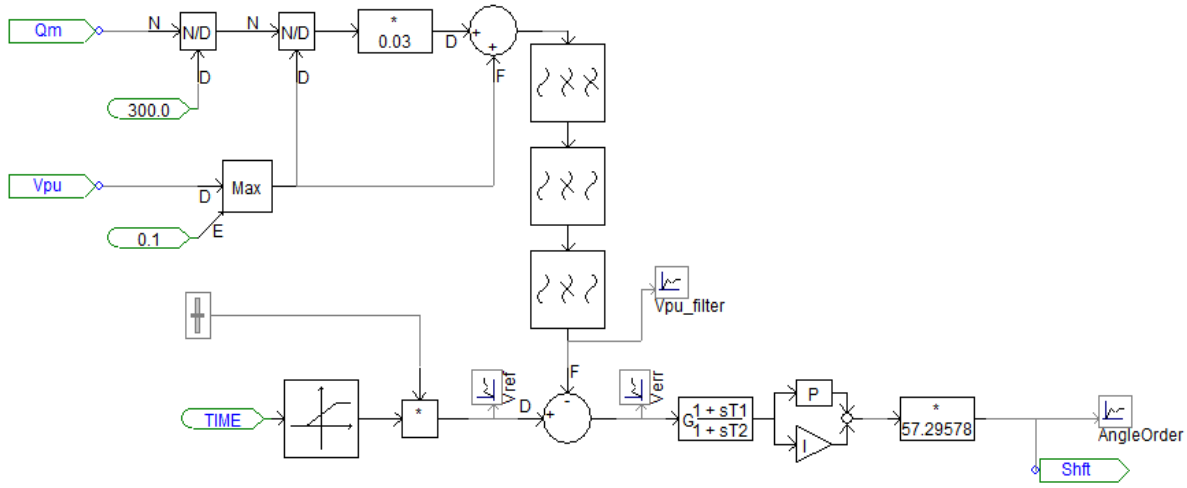

Figure 6. Circuit for generating angle order.

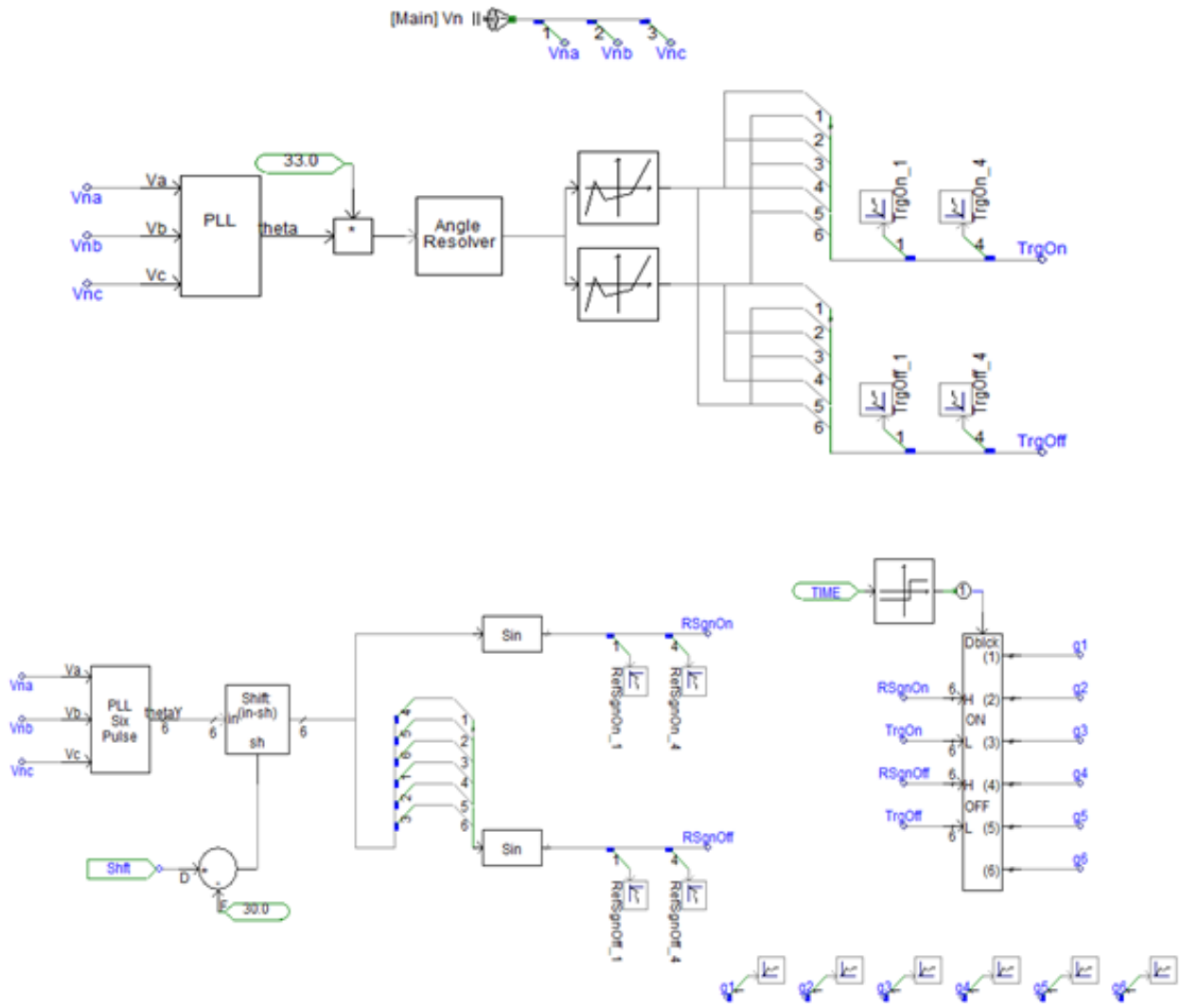

Figure 7. Control circuit for generating pulses.

order required firing signals for the shunt converter is generated.

Measured reactive power and root mean square (RMS) voltage (in per unit) is given as the input. The measured reactive power is divided with the rated reactive power of the circuit. This output is divided with the measured RMS voltage (in per unit). After allowing a drop of about 3% the output of this block is summed up again with the measured RMS voltage. This summed output is passed through filters. The reference voltage (in per unit), is summed with the output signal of the filters. This is given as input to the PI controller. The output of PI controller is the angle order. It represents the required shift between system voltage and voltage generated by shunt converter (STATCOM). This shift determines the direction and amount of power flow. Manual tuning of the proportional and integral gain of the PI controller is done. The output angle order is converted to degrees.

Firing signals are generated by pulse width modulation technique. The instantaneous voltage measured is split into its 3-phase components. This is given as input to the 3-phase PI controlled phase locked loop. It generates a ramp signal that is synchronized in phase to the input voltage signal. This is then multiplied with a real constant to obtain the necessary carrier frequency. From this triangular waveforms synchronized with system AC voltage are generated. Now sinusoidal waveforms synchronized with system AC voltage and shifted by the angle order are to be generated. Again, the instantaneous voltage split into its 3-phase components is given as input to the 3-phase PI controlled phase locked loop. The generated signal that is synchronized in phase to the input voltage signal is shifted by the obtained angle order. Then, this output signal is sent to the sinusoidal function block to generate the required sinusoidal waveforms. The generated triangular and

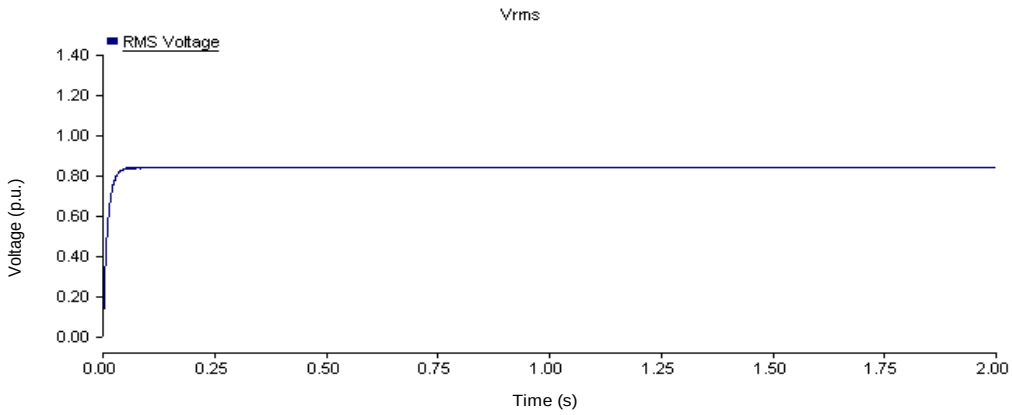

Figure 8. RMS line voltage during normal condition.

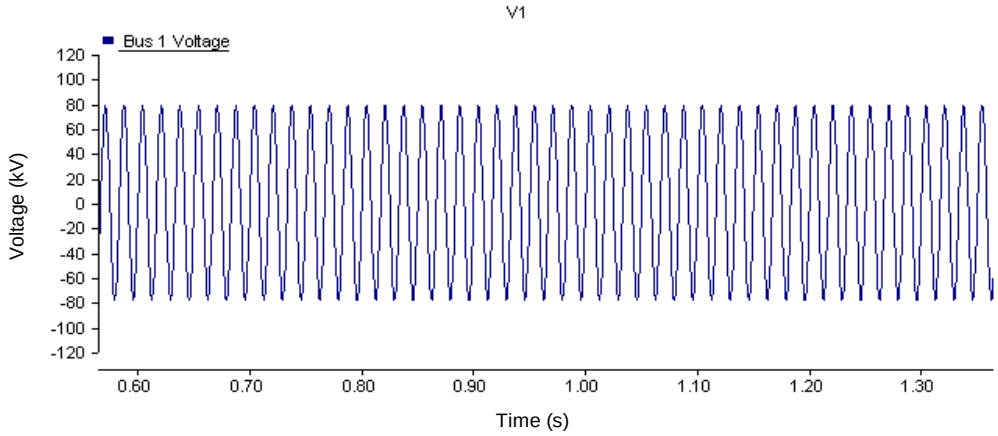

Figure 9. Bus 1 voltage waveform during normal condition.

sinusoidal waveforms are sent to the interpolated firing pulse generation block. Two sets of input signals (reference and triangular ones) are needed; one set for turning on and the second one (a negation of the first set of signals) for turning off. Firing pulses are generated using comparison of sinusoidal signals to triangular signals. The output signals generated are of two element arrays. The first element determines the firing signals which indicate the gate turn-off (GTOs) to turn-on and turn-off. The second element determines the exact moment of switching which is used by interpolation procedure for switching between time steps.

Series converter controller

The controller circuit for the series converter is similar to that of the shunt converter. But here the input values for the generation of angle order are the measured real power and the RMS value of voltage. The generated angle order represents the required shift between system voltage and voltage generated by series converter (SSSC). If the voltage generated by the series converter is in phase with the line current, it exchanges a real power and if the voltage generated by the series converter is in quadrature with line current, it exchanges a reactive power.

TEST CASES AND SIMULATION RESULTS

Five cases were considered to examine the validity of the proposed model. In all the cases, Load 1 is always connected to the system.

Case A

There is no change in load; UPFC is not connected to the system; no transient fault is included in the system. The line voltage, the RMS voltage at Buses 1 and 2 are shown in Figures 8, 9 and 10, respectively under normal operating condition and Table 1 shows the corresponding values.

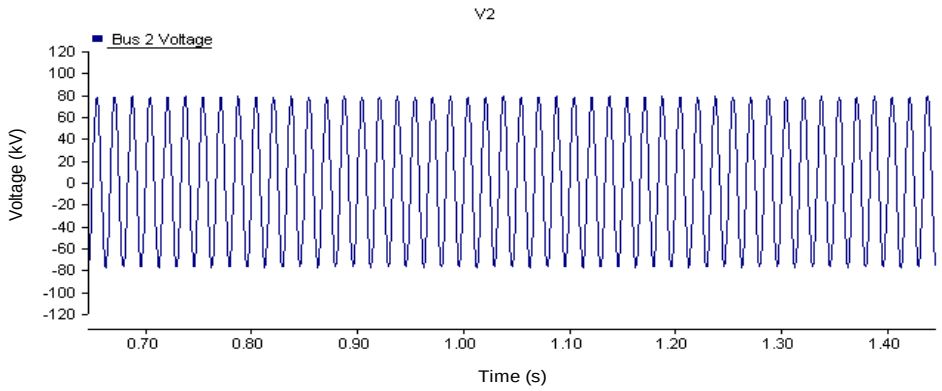

Figure 10. Bus 2 voltage waveform during normal condition.

Table 1. Voltages during increased load and UPFC disconnected condition.

Normal load (only Load 1)			Increased load (Loads 1 and 2) (Time interval of 0.5 to 1 s)		
RMS voltage (pu)	**Bus 1 voltage (kV)**	**Bus 2 voltage (kV)**	**RMS voltage (pu)**	**Bus 1 voltage (kV)**	**Bus 2 voltage (kV)**
0.833	95.53	93.08	0.603	68.58	61.23

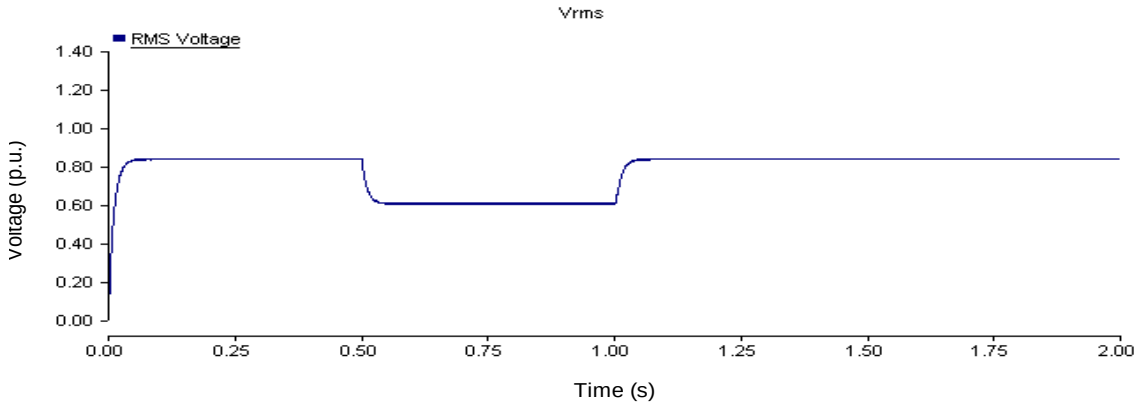

Figure 11. RMS line voltage during increased load.

Case B

There is an increase in system load during the time interval of 0.5 to 1 s; the UPFC is not connected to the system; no transient fault is included. Under this condition, the voltage at the line and bus point drops by as shown in Figures 11, 12 and 13. Voltage drops as much as 23%, giving a V_{rms} value equal to 0.603 p.u. as shown in Table 1.

Case C

There is an increase in system load during the time interval of 0.5 to 1 s; the UPFC is connected to the system; no transient fault is included in the system. From Figures 14, 15 and 16, it is shown that when the UPFC is connected in the system, voltage regulation is done during sudden increased system load conditions. This can be observed from the increase in reactive power during the time interval of 0.5 to 1 s as shown in Figure 17. The normal level of RMS voltage (p.u.) is improved up to a value of 0.976 p.u. from a value of 0.833 p.u. (Case B) as shown in Table 2. So the UPFC improves the initial voltage profile, regulates the voltage during increased system load conditions and the DC capacitor voltage collapse is also avoided (Figure 18).

Case D

There is no increase in system load; the UPFC is not

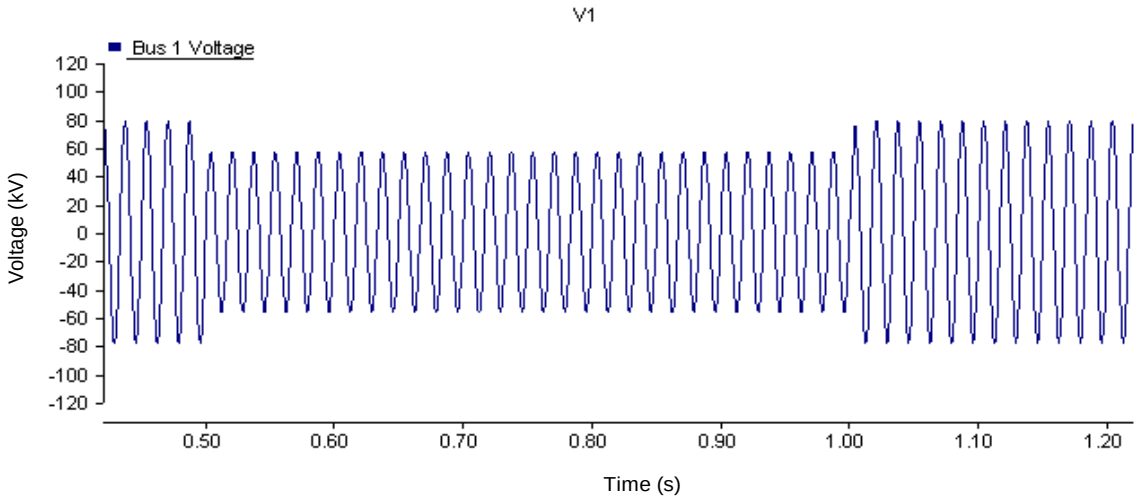

Figure 12. Bus 1 voltage waveform during increased load.

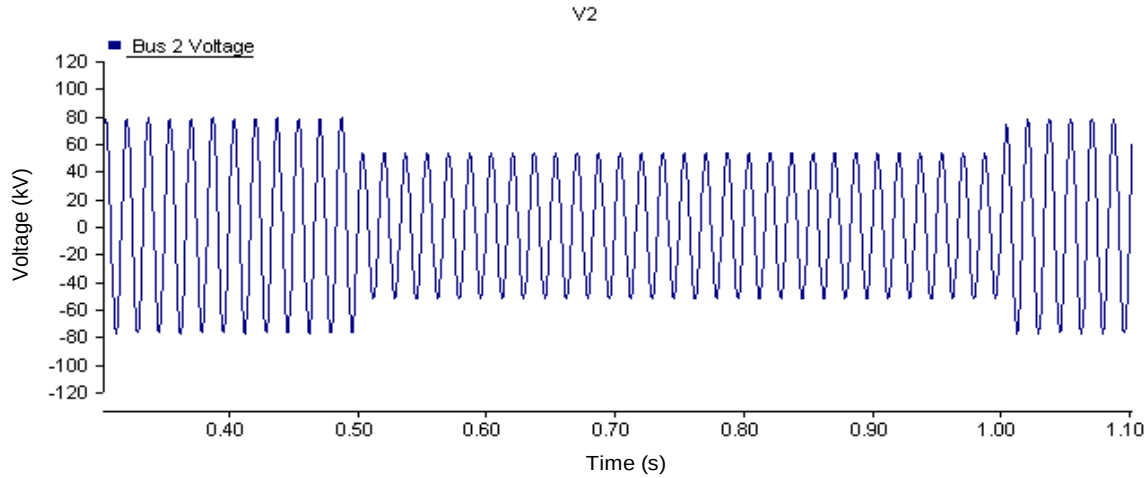

Figure 13. Bus 2 voltage waveform during increased load.

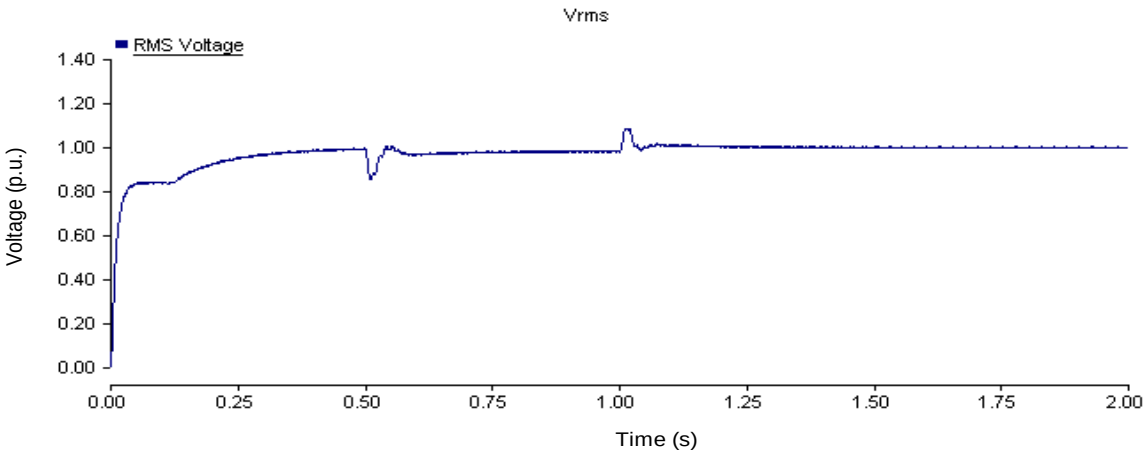

Figure 14. RMS line voltage during increased load and UPFC connected condition.

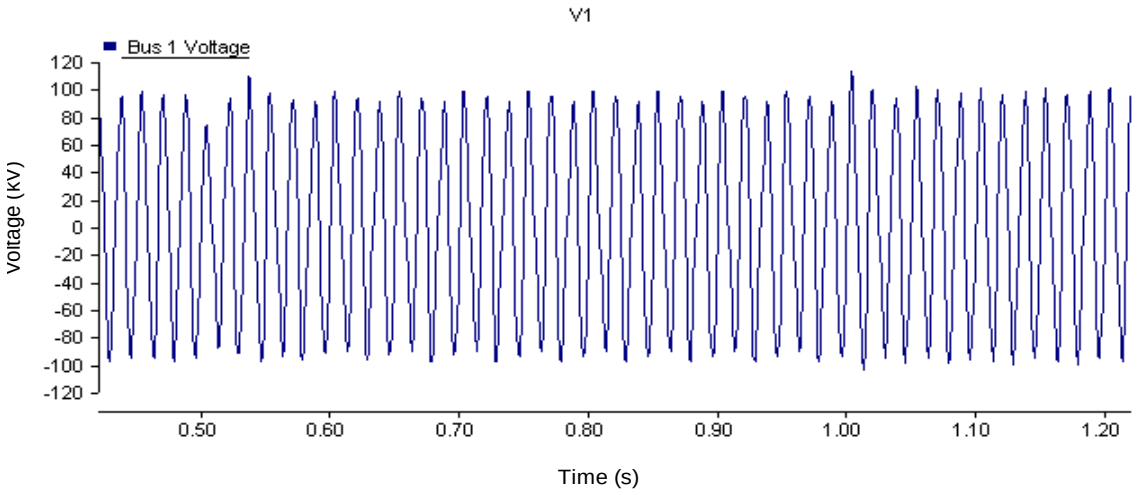

Figure 15. Bus 1 voltage waveform during increased load and UPFC connected condition.

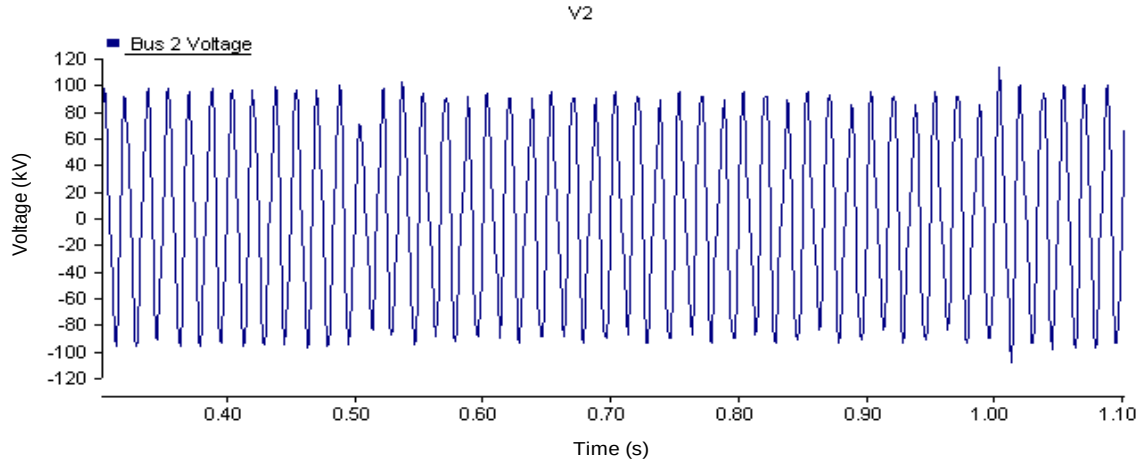

Figure 16. Bus 2 voltage waveform during increased load and UPFC connected condition.

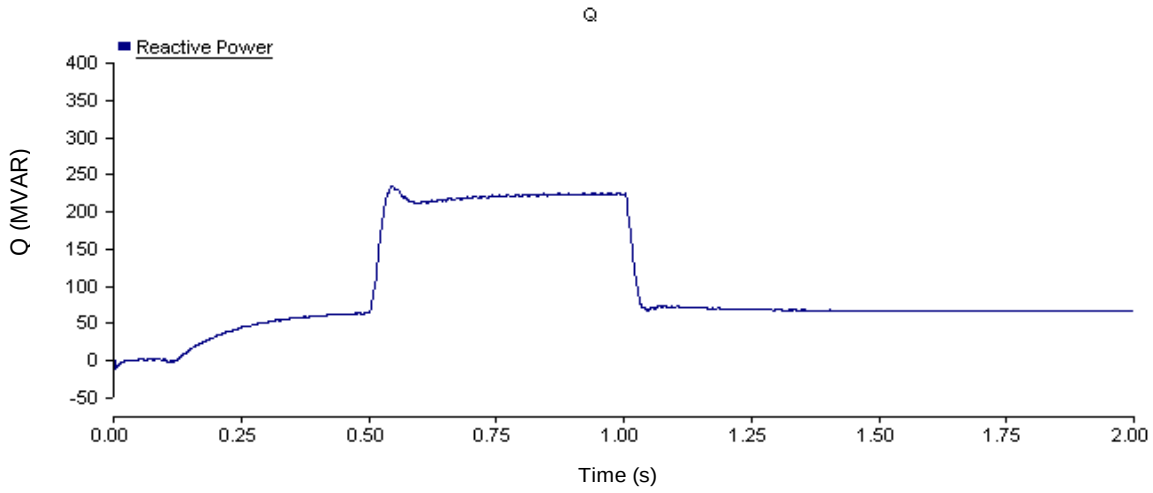

Figure 17. Reactive power waveform during increased load and UPFC connected condition.

Table 2. Voltages during increased load and UPFC connected condition.

Normal load (Only load 1)			Increased load (Loads 1 and 2) (Time interval of 0.5 to 1 s)		
RMS voltage (pu)	**Bus 1 voltage (kV)**	**Bus 2 voltage (kV)**	**RMS voltage (pu)**	**Bus 1 voltage (kV)**	**Bus 2 voltage (kV)**
0.976	112.65	111.45	0.974	107.7	104.10

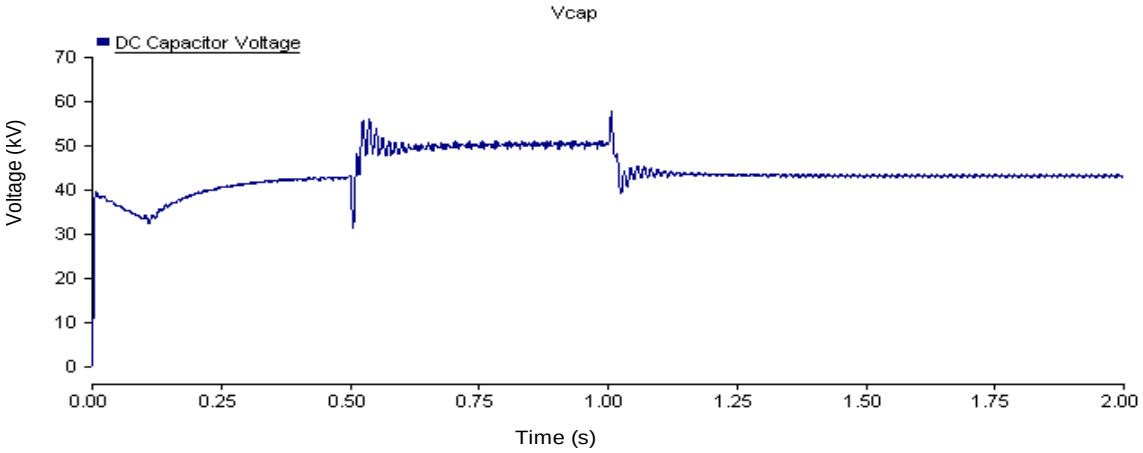

Figure 18. DC capacitor voltage waveform during increased load and UPFC connected condition.

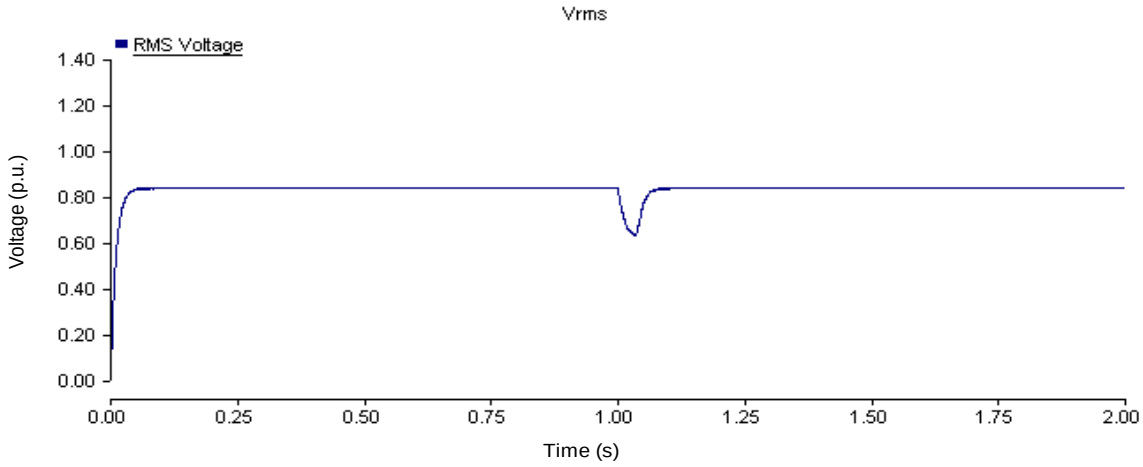

Figure 19. RMS line voltage when transient fault is applied.

connected to the system; a 3-phase transient fault is included during the time interval of 1 to 1.035 s.

From Figures 19, 20 and 21, and Table 3, we get to know that during transient fault conditions the RMS voltage and the two bus voltages are reduced.

Case E

There is no increase in system load; the UPFC is connected to the system; a 3-phase transient fault is included during the time interval of 1 to 1.035 s.

From Figures 22, 23 and 24, and Table 4, it is clear that when the UPFC is connected in the system, voltage regulation is done during transient fault conditions. So the UPFC improves the initial voltage profile, regulates the voltage during transient fault conditions. The DC capacitor voltage collapse is also avoided, as evident from Figure 25. The increased in reactive power support by the UPFC during transient fault is shown in Figure 26. All voltage signals of Buses 1 and 2 voltages displayed in the cases are RMS value of phase A to ground

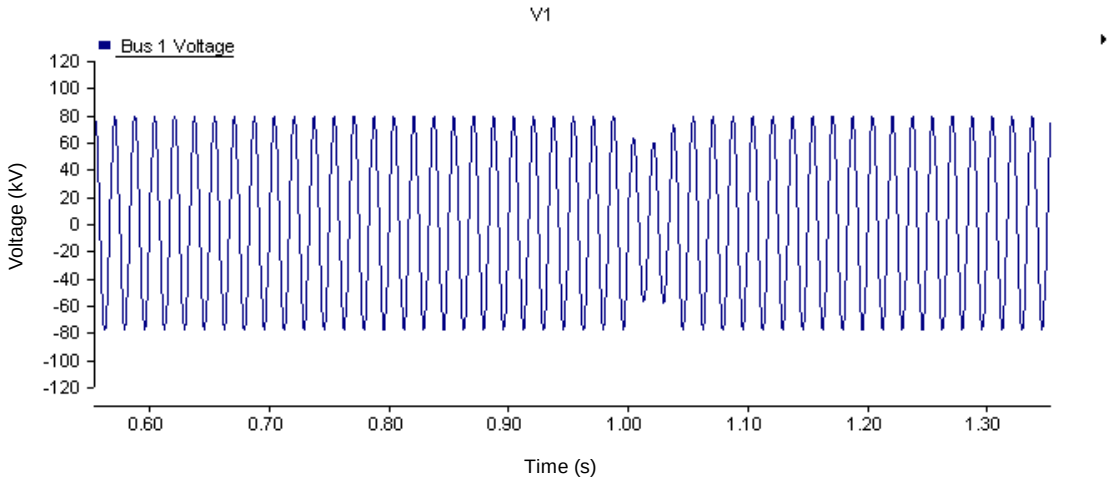

Figure 20. Bus 1 voltage waveform when transient fault is applied.

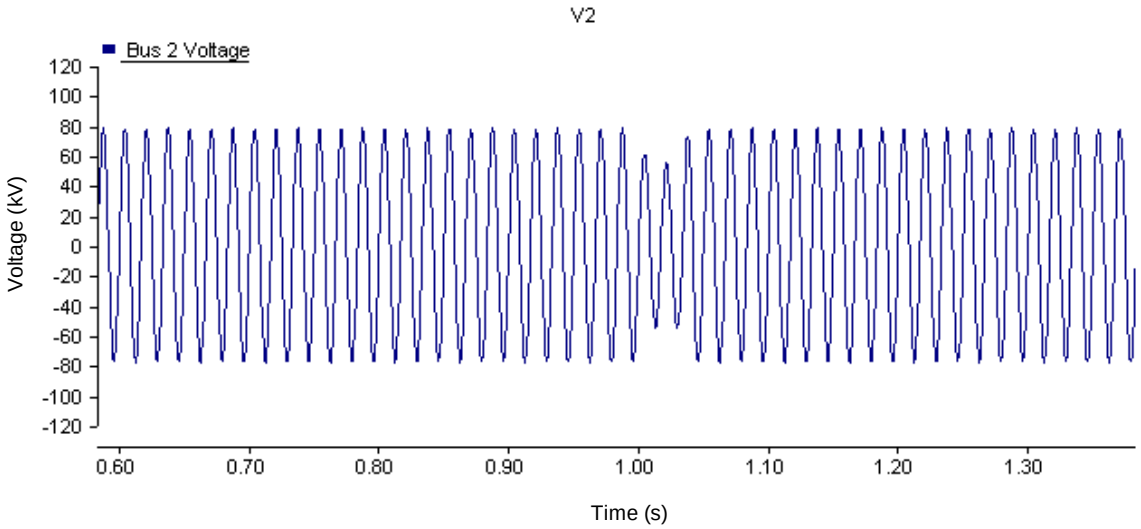

Figure 21. Bus 2 voltage waveform when transient fault is applied.

Table 3. Voltages during transient fault and UPFC disconnected condition.

Without fault			With fault (During 1 to 1.035 s)		
RMS voltage (pu)	**Bus 1 voltage (kV)**	**Bus 2 voltage (kV)**	**RMS voltage (pu)**	**Bus 1 voltage (kV)**	**Bus 2 voltage (kV)**
0.861	95.53	93.08	0.622	70	66

voltage signals.

Conclusion

Due to the sudden increase in the system load or due to certain transient faults, there is a drop in the bus voltages. To regulate the bus voltages, the UPFC is operated in voltage control mode. In this case, the RMS value of voltage (in per unit) is measured simultaneously. When there is a drop in the RMS value of voltage, the UPFC detects it. The necessary firing signals are given to the converters by the controllers. The shunt converter generates or absorbs the necessary amount of reactive

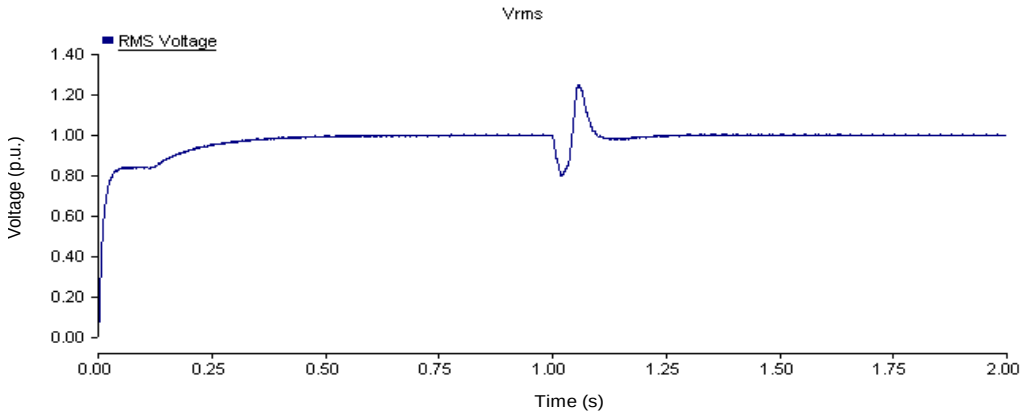

Figure 22. RMS voltage waveform when transient fault is applied and UPFC is connected.

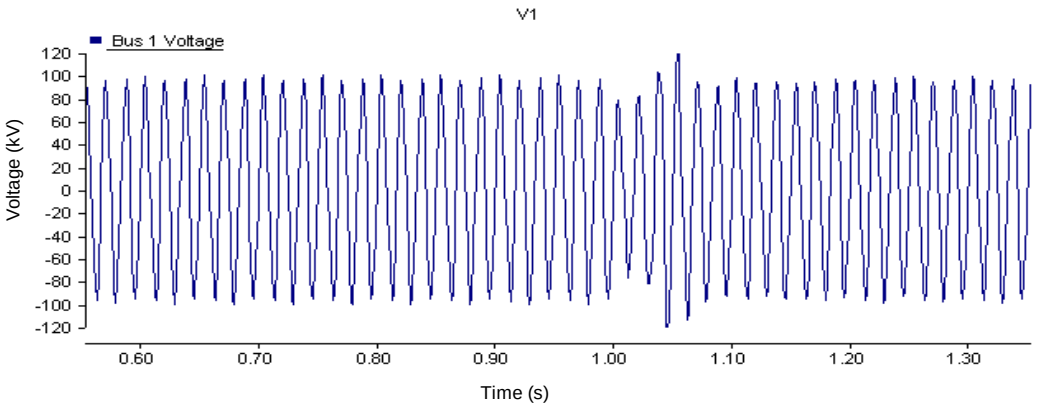

Figure 23. Bus 1 voltage waveform when transient fault is applied and UPFC is connected.

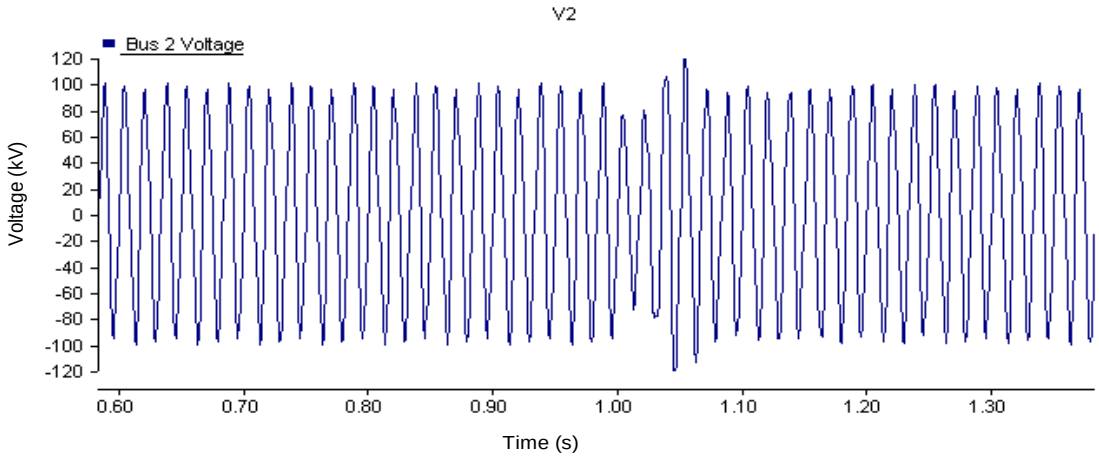

Figure 24. Bus 2 voltage waveform when transient fault is applied and UPFC is connected.

power to regulate the bus voltages. Also, during this operation the collapse of the DC capacitor voltage is avoided. This is done through simultaneous control of the shunt and series converter controllers, through which proper real and reactive power coordination in the UPFC is maintained.

Table 4. Voltages during transient fault and UPFC connected condition.

Without fault			With fault (During 1 to 1.035 s)		
RMS voltage (pu)	**Bus 1 voltage (kV)**	**Bus 2 Voltage (kV)**	**RMS voltage (pu)**	**Bus 1 voltage (kV)**	**Bus 2 voltage (kV)**
0.991	113.9	111.05	0.97	110	107.7

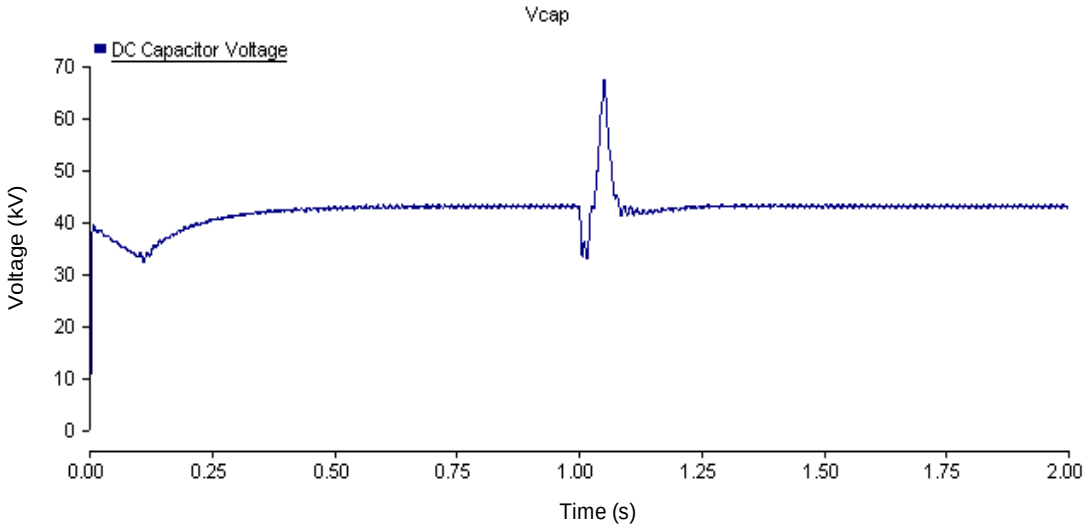

Figure 25. DC capacitor voltage waveform when transient fault is applied and UPFC is connected.

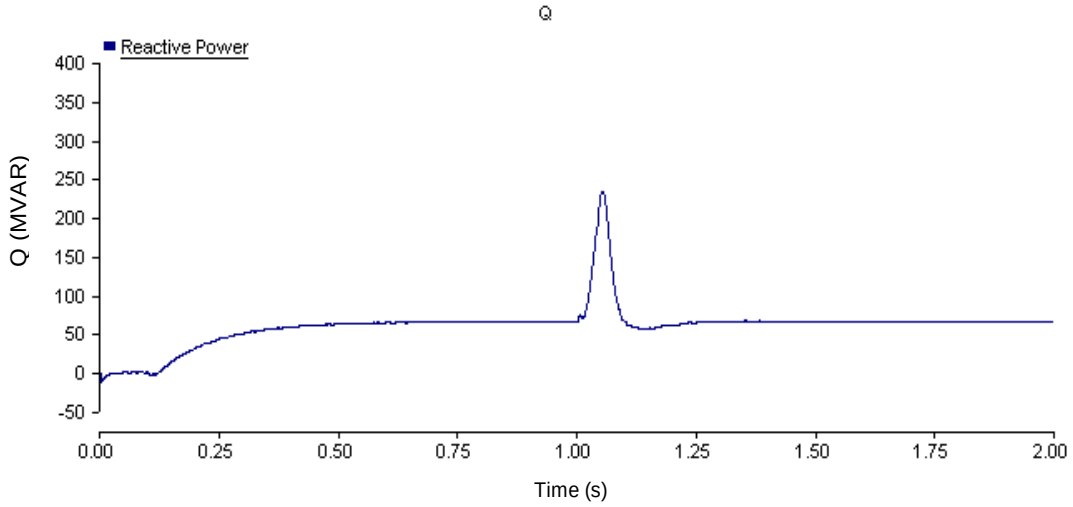

Figure 26. Reactive power waveform when transient fault is applied and UPFC connected condition.

REFERENCES

Acha E, Agelidis VG, Lara OA, Miller THE (2002). Power Electronic Control in Electrical Systems. New. Pow. Eng. Series. First Edition.

Gyugyi L (1992). Unified Power Flow Control Concept for FACTS. IEE Con. Proc. Gen. Trans. Distr. 139(4):323-331.

Hingorani NG, Gyugyi L (2000). Understanding FACTS: Concept and Technology of Flexible AC Transmission System. IEEE Press.

Introduction to PSCAD / EMTDC (2000). Manitoba HVDC Research Centre.

Juan D, José R, Ricardo D (2005). Reactive Power Compensation Technologies: State-of-the-Art Review. Proc. IEEE. 93(12):2144-2164.

Kannan S, Jayaram S, Salama M (2004). Real and reactive power coordination for a unified power flow controller. IEEE Trans. Pow. Syst. 19(3):1454-1461.

Krishna S, Padiyar KR (2005). Discrete control of unified power flow controller for stability improvement. Electric Pow. Sys. Res. 75(2):178-189.

Mohan Mathur TR, Rajiv KV (2002). Thyristor based FACTS Controllers for Electrical Transmission Systems. First Edition, a John Wiley & Sons, Inc. Publication.

Padiyar KR, Kulkurni AM (1998). Control design and simulation of a unified power flow controller. IEEE Trans. Pow. Deliv. 13(4):1348-1354.

Sharma NK, Jagtap PP (2010). Modelling and application of Unified Power Flow Controller (UPFC). IEEE Third Int. Con. Emerging Trends Eng. Technol. 93(12):2144-2164.