

Full Length Research Paper

5 nm gap via conventional photolithography and pattern-size reduction technique

Th. S. Dhahi^{1*}, M. E. Ali¹, U. Hashim^{1,2}, Ala'eddin A. Saif² and T. Nazwa¹

¹Institute of Nano Electronic Engineering, Universiti Malaysia Perlis, 01000 Kangar, Perlis, Malaysia.

²School of Microelectronic Engineering, Universiti Malaysia Perlis, 01000 Kangar, Perlis, Malaysia.

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A simple method for the fabrication of nanogaps of less than 6 nm by conventional photolithography combined with patterned-size reduction technique is presented. The method is based on the complete conversion of a photolithographically embedded polysilicon structure on a silicon wafer into a semiconductor oxide layer and subsequent stripping of the oxide layer by etching with a buffer oxide etching (BOE) solution. With this technique, there are no principal limitations to fabricate nanostructures with different layouts and dimensions along with an improved pattern size resolution. The method is demonstrated by preparing self-aligned nanogaps of 5–6 nm dimensions on a Si–SiO₂ substrate. Polysilicon material is used to fabricate the nanogap structure and gold is used for the electrodes. Two chrome masks are used to complete this work. The first one is for the nanogap pattern and the second one is for the pad electrode. The fabricated structure is optically and electrically characterized with a field emission scanning electron microscope (FESEM) and dielectric analyzer (DA).

Key words: Nanogap, photolithography, pattern-size reduction, wet etching, optical and electrical characterization.

INTRODUCTION

The evolution of semiconductor devices into nano-regime has tempted researchers to look into nano-patterning techniques in order to understand the effects and properties at nanometer scales. Miniaturization based on optical lithography wavelength reduction has already hit a roadblock and the changeover to newer technologies is not financially viable for smaller manufacturers. The ability to create sub-lithographic nm-scale features without the need of high-end lithography tools will create new opportunities for the electronics industry. Thus, a reliable technique to fabricate nanometer-sized structures is required for the realization of next generation nano-electronic devices. Some of the present inventions relate to a process of creating an electrode with a nanogap. The development of easy, low-cost and high-throughput techniques for the fabrication of nanostructures has been of great interest for both the possibility to increase the

device-packing density and for reducing the power consumption, as well as for the creation of a new class of nano-electronic devices, such as, single electron transistors (Namatsu et al., 2003) metal/insulator tunnel transistors (Sasajima et al., 1999), nanowire transistors (Marchi et al., 2006), nanotube- or nanoparticle-based devices (Allen and Kichambare, 2007; Ding et al., 2006). Chemical and biological nanosensors, biochips and nanobioelectronics are among the others progressing rapidly (Schoning and Poghossian, 2006; Yogeswaren and Chen, 2008, Yih and Talpasanu, 2008, Poghossian et al., 2006).

A coupling of biorecognition elements with nanomaterials (nanoparticles, nanotubes, etc.) and nanostructures (e.g., nanoelectrodes, nanotransistors, nanogaps, nanopores, nanochannels) of comparable dimensions might allow the creation of hybrid systems with unique functional and application possibilities (Tang et al., 2006; Zhang et al., 2008; Sigalov et al., 2008; Gun et al., 2008; Tsai et al., 2005; Liang and Chou, 2008; Cho et al., 2008). Such functional hybrid systems (that is, the “marriage” of biomolecules and nano-scaled transducers)

*Corresponding author. E-mail: sthikra@yahoo.com.

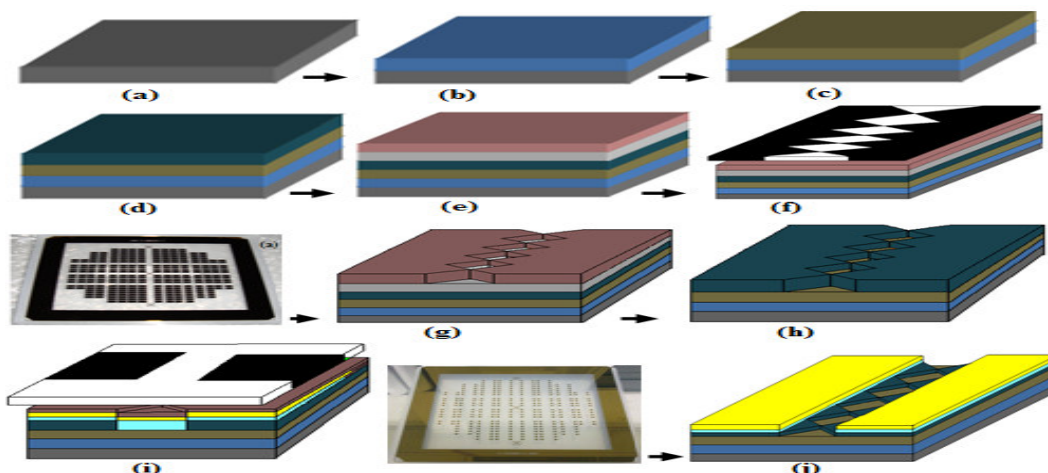


Figure 1. The fabrication process flow of the polysilicon nanogap structure. Shown are (a) starting material (silicon wafer) (b) a deposit of 50-nm SiO_2 layer (c) 150-nm Si_3N_4 layer (d) 600-nm polysilicon layer (e) photoresist coating (f) mask1 exposure (g) resist development (h) dry etching of the polysilicon layer (i) exposure to mask2 after depositing Ti/Au layer (j) and the final device after applying wet etching for the Ti/Au layer.

provide powerful tools, not only for manipulation and detection, but also for the fundamental research of single biological molecules (DNA immunospecies, proteins, etc.) and living cells. The realization of different nanometer-sized structures has been demonstrated by advanced high-resolution nanolithographic techniques such as electron- or ion-beam lithography, focused ion-beam milling, scanning tunneling or atomic force microscopy, nanoimprint lithography, and different top-down fabrication techniques, etc. (Chen and Pepin, 2001). Although these techniques provide high resolution in generating different nanostructures, most of them are time-consuming, low-throughput, complicated and expensive. If conventional photolithography could be applied to form nanometer-sized structures including line and space patterns, it would be highly advantageous. Therefore, recently, some non-conventional techniques in combination with conventional photolithography have been proposed for the preparation of nanoelectrodes, nanogaps and other nano-scaled devices. These techniques include, for instance, a photoresist thermal reflow and shrinking (Meng et al., 2001) or photoresist ashing technique (Kim et al., 2008), a shadow evaporation process (Ishida et al., 2005), a controlled size-reduction using the oxidation of Si (Choi et al., 2003; Hashioka et al., 2005; Cho et al., 2007) or laser-assisted electrochemical etching (Juhász and Linnros, 2002), chemical-mechanical polishing (Lee, 2003), the decrease of separation between metallic electrodes by means of an electro-deposition from an electrolyte solution (Morpurgo et al., 1999), methods that utilize a sidewall structure (Chung et al., 2002), a self-aligned plasma etching of a silicon dioxide layer and silicon substrate (Georgiev et al., 2003), or a lateral, partial anodic oxidation of the side-

edge of a photolithographically-structured metallic film (Hashioka et al., 2003), techniques that use a silicon-on-insulator structure (Strobel et al., 2007), etc.

An alternative solution for the fabrication of self-aligned nanostructures by means of conventional photolithography combined with pattern-size reduction techniques has recently been proposed (Platen et al., 2006; Poghosian et al., 2005). The method of thermal oxidation is experimentally demonstrated by patterning nanostructures with different sizes and layouts on a polysilicon material. The feasibility of the proposed method for the preparation of polysilicon nanogaps of less than 6 nm on a $\text{Si}_3\text{N}_4\text{-SiO}_2\text{-Si}$ substrate presented. A number of methods for fabricating nanogaps have already been established. But our goal is to develop a least cost method of fabrication that can be applied in batch production of desired nanogap electrodes.

PROCESS DESIGN

In this work, a silicon substrate is used to fabricate the nanogap structure. The first step is to design and produce a mask. We use two masks: one for the polysilicon nanogap and other for the gold electrodes. Dry etching by RIE (reactive ion etching) is used to produce the polysilicon nanogap and wet etching is used for the gold electrode structure.

The starting material used in this project is a p-type, 100 mm in diameter (4-inch) silicon substrate wafer. As for the lithography process, two photomasks are employed to pattern the nanogap by conventional photolithography and dry etching techniques. Commercial chrome masks are used in this research for a better photomasking purpose.

The fabrication process flow is schematically depicted in Figure 1. As described by Dhahi et al. (2010), the process essentially consists of: (1) deposition of a low stress thin film of $\text{Si}_3\text{N}_4\text{-SiO}_2$ on silicon wafer by PECVD followed by the deposition of a 600 nm

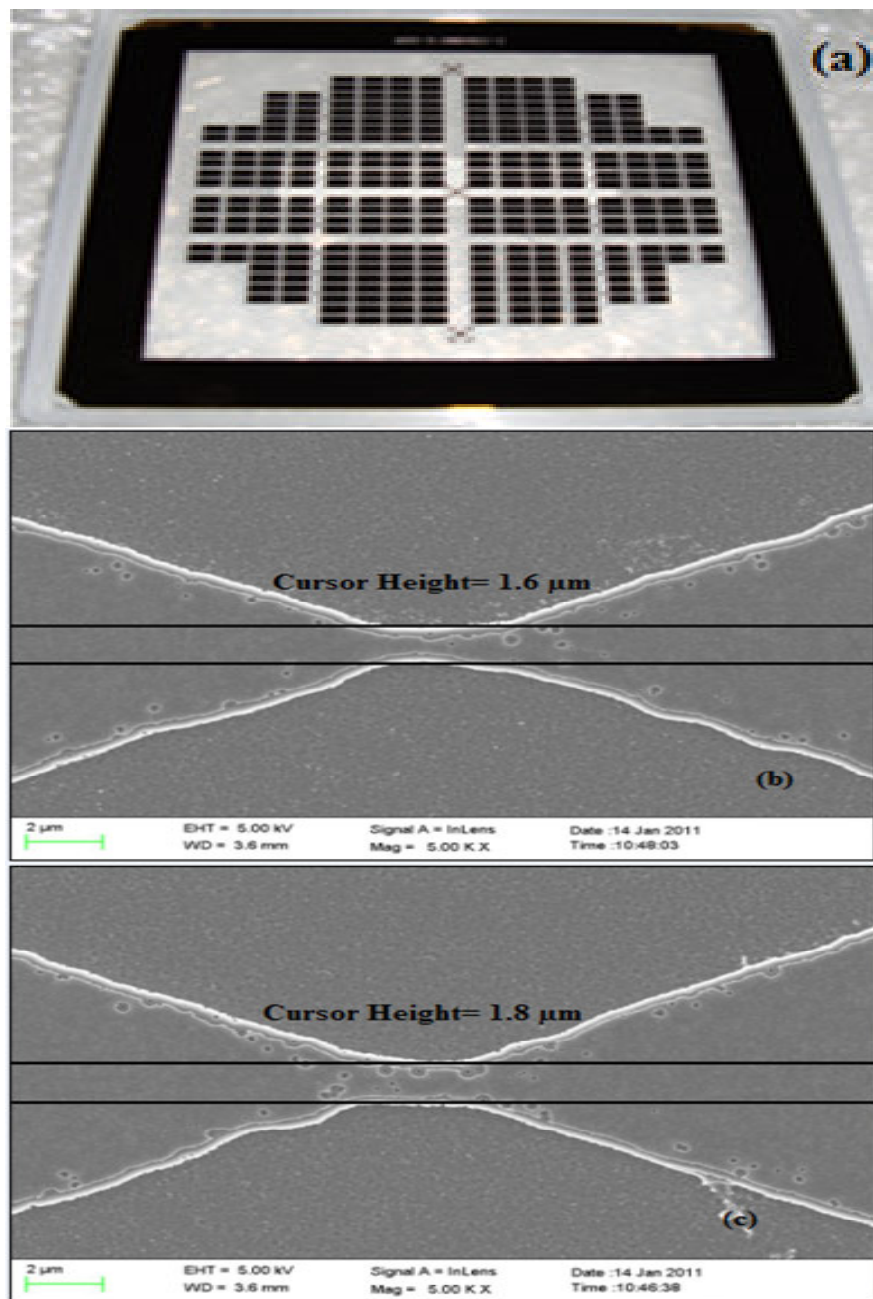


Figure 2. (a) Photo mask and FESEM images of fabricated polysilicon pattern (b) before and (c) after the thermal oxidation process.

polysilicon layer by LPCVD (Figure 1(d)); (2) patterning the nanogap structure by moving the structure from chrome mask to polysilicon layer using UV-lithography process (Figure 1(f)); (3) dry etching of the polysilicon layer using RIE process after developing the resist (Figure 1(h)); (4) application of size reduction technique using dry oxidation process to pattern the nanogap structure (analyzed in “Results and Discussion”); (5) deposition of Ti/Au layer to fabricate the pads electrodes and finally, (6) patterning the electrodes pad to characterize the device electrically (Figure 1(j)).

The structured polysilicon layer was oxidized at 1000°C in dry O₂ to form the oxide layer of silicon dioxide (SiO₂). The oxidation time

was from 20 to 90 min depending on the thickness of the polysilicon layer. The prepared structures are characterized before and after the oxidation process by means of a Field Emission Scanning Electron Microscope (ZEISS FESEM ULTRA55).

RESULTS AND DISCUSSION

Figure 2 shows (a) the photo mask and, (b and c) the FESEM cross-sectional view of an original photo

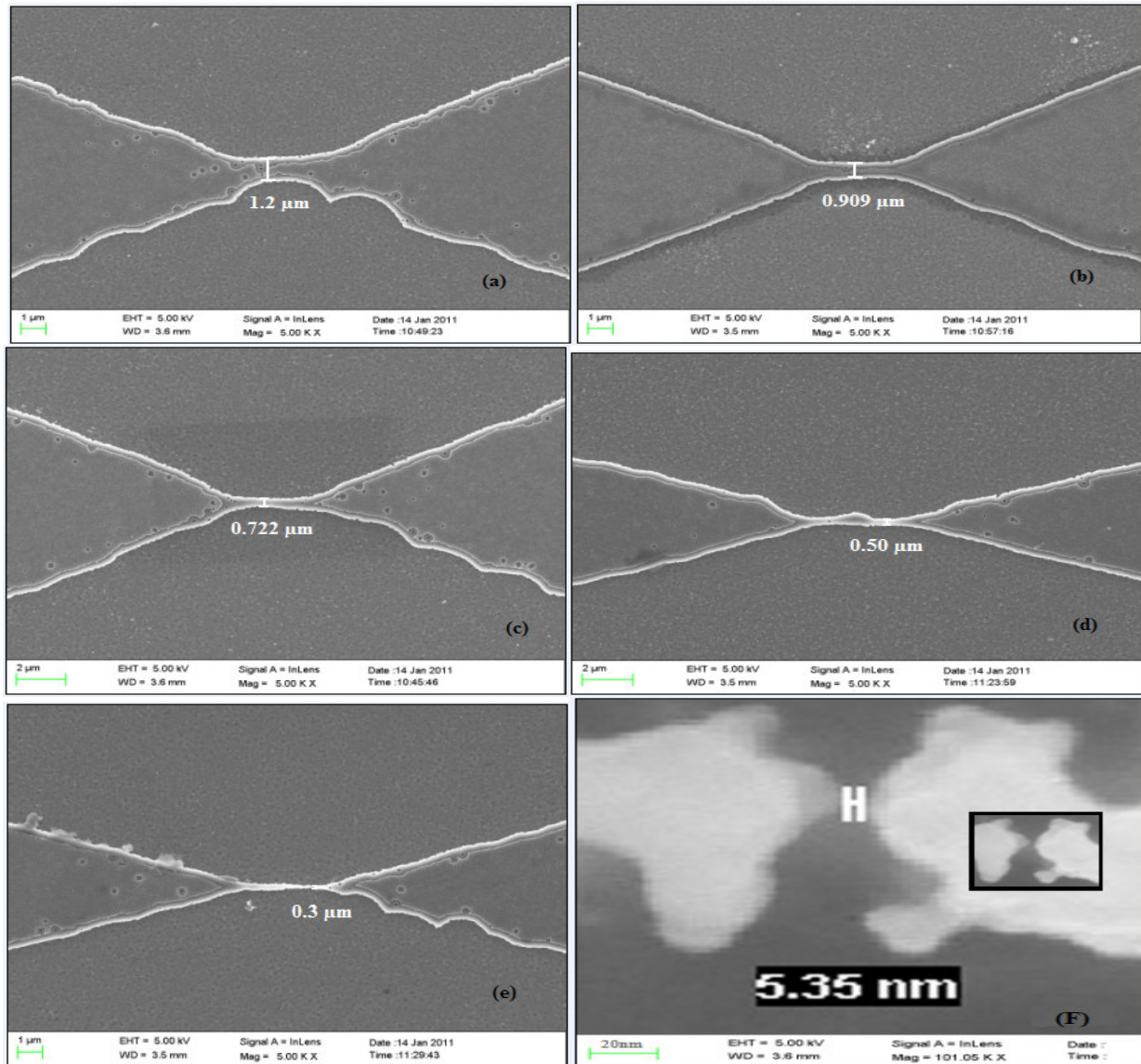


Figure 3. FESEM images showing ((a) – (e)) the pattern thickness and (f) fabricated nanogap, at the end of sequential oxidation and etching. The images are at the end of (a) 20 min (b) 40 min (c) 60 min (d) 70 min (e) 80 min, and (f) 90 min cyclic oxidation and BOE etching.

lithographically-patterned polysilicon layer before and after the application of the oxidation process.

After exposing the chrome mask (Figure 2(a)), the pattern of the original 600 nm thick polysilicon layer is laterally expanded from 1.6 μm (Figure 2(b)) to 1.8 μm (Figure 2(c)) by the oxidation at 1000°C for about 20 min. The subsequent etching and stripping of the oxide layer by BOE solution reduces the pattern thickness from 1.8 to 1.2 μm ((Figure 3 (a)). Thus the original pattern reduction of 400 nm (1.6- 1.2 μm) is achieved in the first round of alternate oxidation and etching.

The precise control of nanostructure dimensions is a crucial point for a reproducible fabrication. The layer-reduction or pattern size reduction technique can

generate an excellent reproducibility in controlling the layer diminution after the oxidation of the semiconductor layer, owing to the nature of the thermal oxidation process. Thus, the nanogap size can be precisely controlled by the oxidation conditions (temperature and time) as well as by the thickness of the semiconductor layer. In order to investigate dependence of the pattern-size reduction on the oxidation time of the patterned polysilicon layer, the FESEM photographs of the prepared nanogap structures are made after each 20 min of oxidation for the first three rounds of oxidation and etching (Figure 3, (a) – (c)) and then the oxidation time of each of the next three cycles is reduced to 10 min ((d) – (f)). Figure 3 ((a) - (f)) demonstrates FESEM photographs

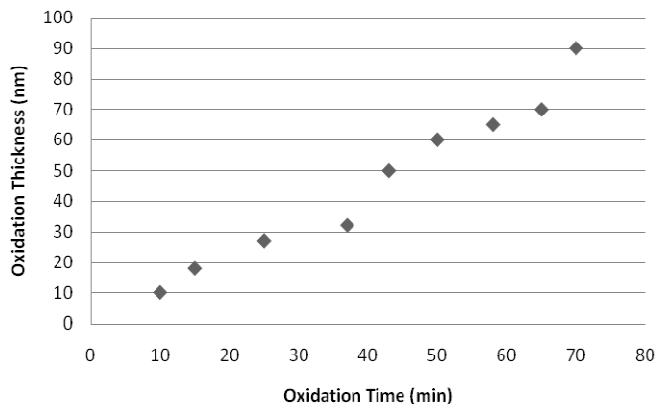


Figure 4. The relationship of oxidation thickness (y-axis) with the cumulative oxidation time (x-axis).

of a patterned polysilicon layer after each round of thermal oxidation and etching.

In this experiment, the original (photolithographically-patterned) gap size before the oxidation and etching is zero. With the increment of the oxidation time and subsequent BOE etching, the pattern height is decreased. We carefully control the oxidation time and realize a gap size of 5 nm at the end of 6th cycle (a cumulative oxidation time of 90 min) (Figure 3 (f)). Further increasing of the oxidation time does not lead to a significant reduction of the gap size. This means that after 90 min of oxidation, the polysilicon layer is completely oxidized and stripped out producing a gap.

In this research, the dry oxidation process (oxygen source is dry O_2) is applied for the thermal oxidation of the deposited polysilicon layer. After controlling a number of factors such as temperature, pressure, dopant type and concentration of the Si-crystal orientation), the oxidation growth rate can be defined. When the oxygen starts to react with the polysilicon, it forms a silicon dioxide (SiO_2) layer, which shields the silicon atoms on the polysilicon structure from the incoming oxygen molecules. At the beginning of oxide formation, the oxide layer is very thin (<200 nm) and oxygen molecules can penetrate the oxide layer with few collisions to reach the polysilicon layer to oxidize them continuously increasing thickness of the silicon dioxide layer. Thus a proportional relationship is observed when oxidation thickness is plotted against oxidation time (Figure 4).

The oxide thickness is controlled within the range 200 nm to avoid excessive consumption of the top polysilicon layer during the oxidation and etching process. Berg et al. (2005) also observed that increasing oxidation time increases in the oxidation thickness, strongly supporting our findings.

Oxidation time also directly affects the size of the gap. This is clearly reflected by a plot of gap-size versus time of thermal oxidation (Figure 5) which also shows a proportional relationship.

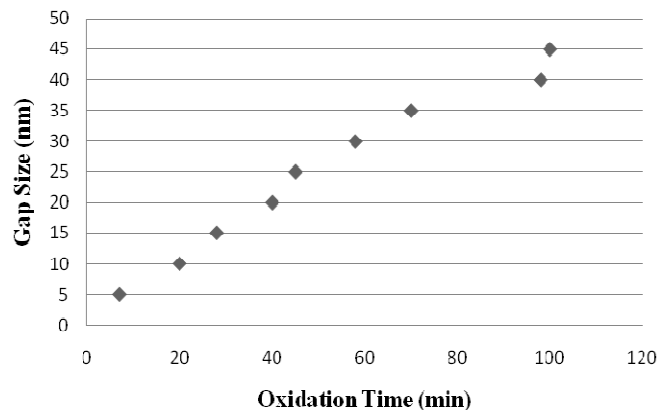


Figure 5. The relationship of gap-size (y-axis) with the cumulative oxidation time (x-axis).

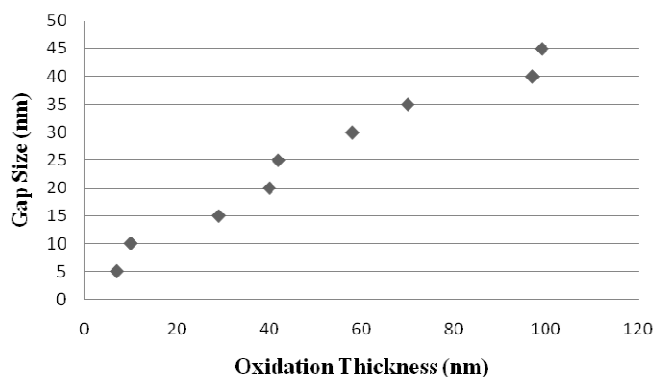


Figure 6. The relationship of gap-size (y-axis) with the cumulative oxide layer thickness (x-axis).

After the application of wet etching with a BOE solution to remove the oxide layer where the silicon atoms are attached with the oxygen atoms, the thickness of the polysilicon layer decreases and the size of the gap increases. Thus a proportional relationship appears between gap-size and oxide-layer thickness (Figure 6).

The size reduction technique starts with the growth of oxide layer. The thickness of the polysilicon consumed is approximately 99% of the total oxide layer thickness. This means that for every 10 nm of the oxide layer growth, 10 nm of the polysilicon layer is consumed. The sample is then dipped into the BOE solution to remove the entire oxide layer. The detailed dimensions for the size reduction of the polysilicon layer are shown in FESEM images (Figure 3). After each oxidation and etching steps, the cursor height decreases from 100 to 400 nm. This is reasonable because the oxide is consumed from the right and left side of the polysilicon nano-gap structures.

The electrical characterization for the nanogap structure is necessary to evaluate the potentials benefits

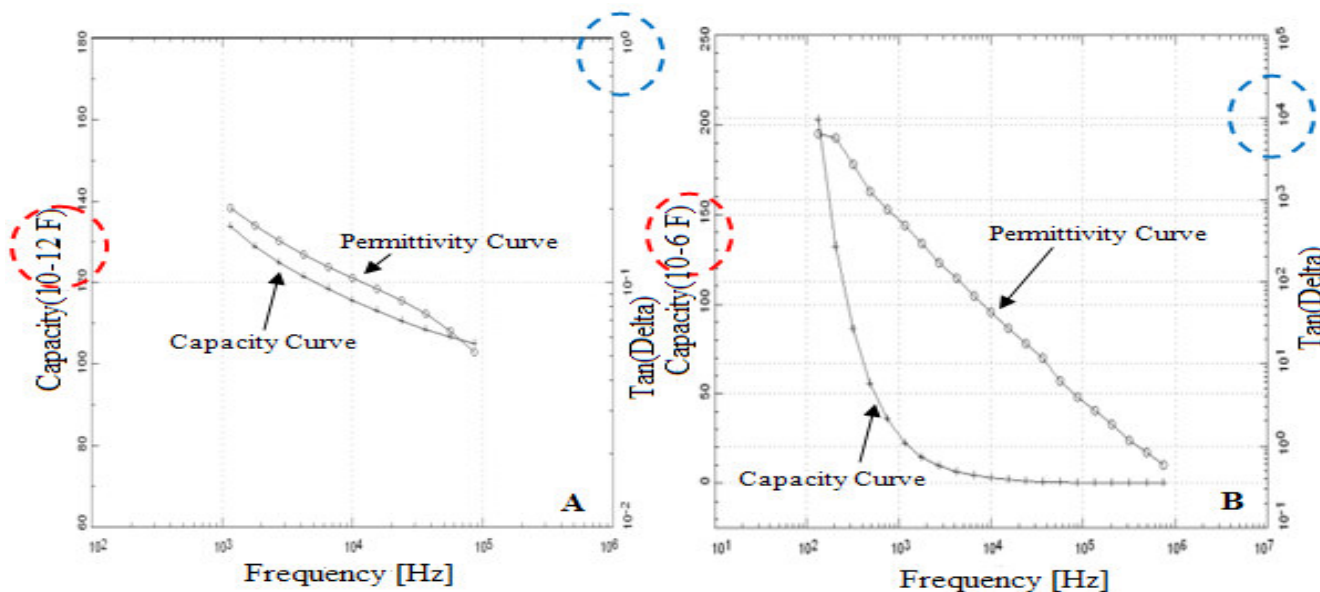


Figure 7. Capacitance and permittivity profile of the fabricated 5 nm gap structure (a) and a zero-gap structure before thermal oxidation (b) as function of frequency.

and application of the fabricated nanogap structure. A nanogap structure is expected to consume less power in the operation of electrical devices. Thus a measurement of permittivity, capacitance and conductivity should provide valuable information.

The studies of the dielectric properties are another important source of information about conduction processes since it can be used to understand the origin of the capacitance value in the nanogaps structures. According to Anantha et al. (2005), the dielectric permittivity can be expressed in term of the capacitance by the following equation:

$$C = \epsilon \cdot A / d \dots \tag{1}$$

Where: $\epsilon = \epsilon / \epsilon^0$

ϵ : the permittivity

ϵ^0 : the permittivity for free space

C: the capacitance value

A: the area of the nanogap structure

d: the size of the gap

Figure 7 shows the capacitance as well the permittivity $\{\epsilon \cong \text{Tan}(\Delta)\}$ curves of (a) a 5-nm gap and (b) a zero/no-gap structures as a function of frequency. It is observed that the value of the capacitance and permittivity of both structures decreases as the frequency increases (Ala'eddin et al., 2011). At 5.35 nm gap Figure 7(a), the capacitance and the permittivity values was very small ($C \cdot 10^{-12}$ F, $\epsilon < 1$). Because of the air between two electrodes, the permittivity cannot increase more than unity. And because the size of the gap is very small and

the area of the electrodes is decreased after using size reduction technique respectively (Dhahi et al., 2011), the capacitance is decreased gradually as the frequency increases.

On the other hand, at zero gap (Figure 7(b)), it is observed that capacitance measurement is higher ($C \cdot 10^{-12}$, $\epsilon > 1$) than nanogap because the gap size between the electrode is zero and the area of the electrode is bigger before using thermal oxidation process. This can also be explained from Equation 1. Putting a value of zero in the denominator ($d = 0$), makes the capacitance infinite. In the other sense, the permittivity of the polysilicon materials is higher than the air. Comparative studies with different nano-gap size structures are necessary to draw a solid decision of the potential benefits of the fabricated nano-gap structures. Our research group is working on these issues and will be reported it in separate publications.

Commonly, the capacitance and permittivity decrease is attributed to the increases in frequency. The capacity decreases as small size of gap and the permittivity follow the same trends of the capacitance behavior.

$$C = 1/2\pi Rf \dots \tag{2}$$

Where: R: the resistivity, f: the frequency

The study of frequency dependent conductivity is a well established method for characterizing the hopping dynamics of the charge carrier/ions (Roya et al., 2004). Figure 8 shows typical frequency dependence of AC conductivity of 5.35-nm gap electrodes. The frequency dependence of AC conductivity is usually characterized

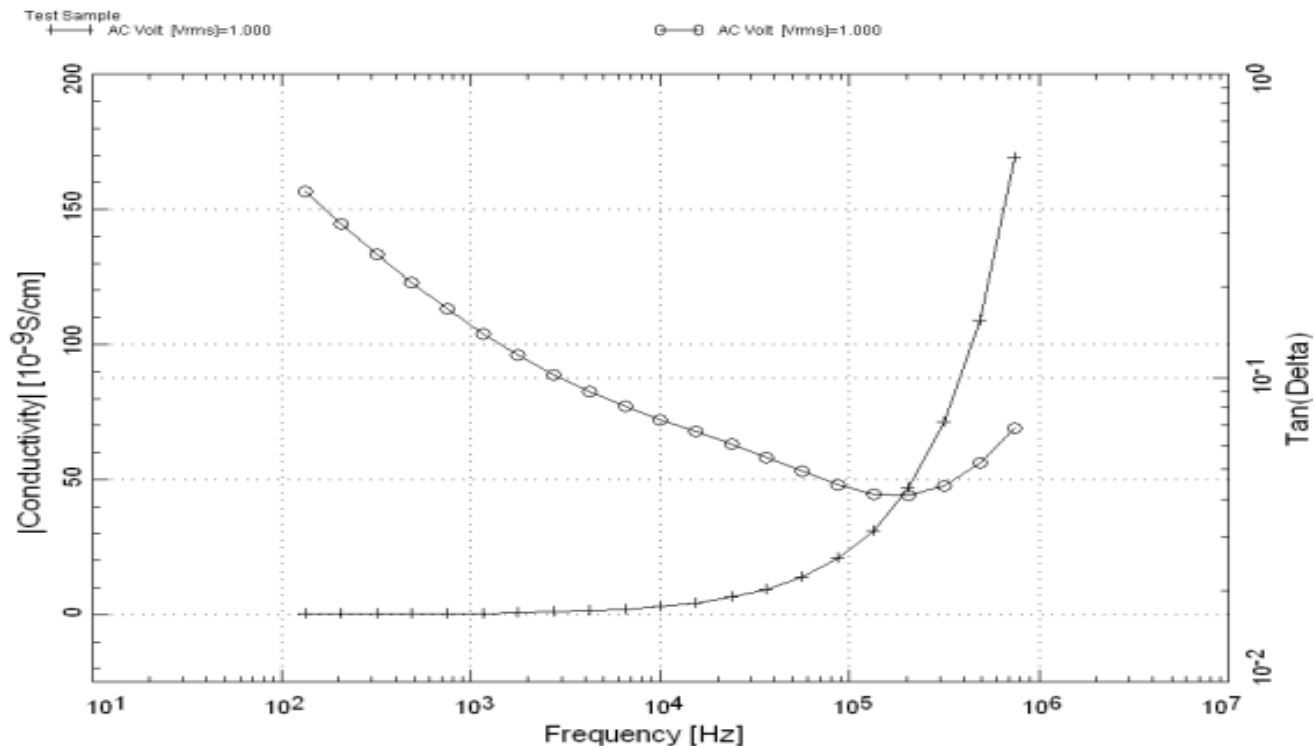


Figure 8. Conductivity profile of 5 nm gap structure as a function of frequency.

by a power law described in bibliography (Muralidharan et al., 2004; Mahboob et al., 2006; Oueslati et al., 2010).

Figure 8 show the conductivity value increase gradually with the frequency. When the charges oscillation mean increases, the contact between them gradually increases increasing the conductivity between the electrodes. The resistivity automatically decreases with the increment of conductivity.

Conclusion

A simple method for the fabrication of nanogap of less than 6 nm in dimensions on polysilicon-coated silicon substrate is demonstrated. The method avoided the use of complicated nanolithography techniques to produce such gaps. It combines conventional photolithography with pattern-size reduction techniques and is based on the reduction of the pattern semiconductor height using alternate thermal oxidation and etching. The proposed method is demonstrated by preparing lateral nanogaps of 5-6 nm dimensions. By using thicker polysilicon layer, the gap-size can be further reduced. Gap-size reduction has potential benefits in electrical devices that can be operated by a low level of power supply. This was confirmed by measuring capacity, permittivity and conductivity profiles of the fabricated structure. A more solid decision can be drawn by measuring the electrical properties of nanogaps with different dimensions. Future

experiments will focus on building up nanobiosensors by coupling biomolecules within the nanogaps with dimensions close to their persistence length.

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