Full Length Research Paper

Look ahead dynamic threshold voltage control for enhanced write margin of 45 NM 7T-SRAM cell

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Instability of SRAM memory cells derived from aggressive technology scaling has recently been one of the most significant issues. Although a 7T–SRAM cell with an area tolerable separated read port improves read margins even at sub-1V, it unfortunately results in degradation of write margins. A new memory cell adopting a look ahead body-bias which dynamically controls the threshold voltage was proposed in order to assist the write operation. Simulation results have shown improvement in both the write margins and access time.

Key words: Body-bias, SRAM, low power design.

INTRODUCTION

In a previous scenario of SRAM development, technology scaling had been able to achieve higher performance, larger memory capacity and lower power consumption at the same time so far. However, when it comes to a sub-100 nm era, an unexpected random variation in the threshold voltage (Vth) derived from the process variation and the lowered supply voltage significantly deteriorates the stability of SRAM memory cells. Then, we propose a 7T-SRAM cell adopting the active body-biasing control on PD-SOI, where the Vth of each transistor can be dynamically controlled through direct body contact (Hirano et al., 2010, 2008). Here, the HTI (Hybrid Trench Isolation) technology shown in Figure 1 drastically reduces the area penalty and parasitic gate capacitance to almost the same level as bulk MOSFETs. For SRAM memory cells, the use of word / bit line signals as the body-biasing control signals for memory cells improves both the write margins and access time.

IMPROVED WRITE MARGIN BY LOOK AHEAD DYNAMIC THRESHOLD VOLTAGE CONTROL

In general SRAM memory cells, conflicting requirements for improving the write and read margins simultaneously has been

posing significant design challenges in low voltage operation. Although previous work by Chang et al. (2005) on 8T-SRAM and 7T-separated read port expands the read.

According to Suzuki et al. (2006), SRAM with margins result in the degradation of additional transistors of the write margins. In addition, 7T-SRAM memory cells using a single bit-line alone deteriorate both the access time and write margins especially in the '1'-write mode due to the threshold voltage loss of access transistor. Even though boosting VSS nodes in the memory cell suppress the degradation of write margins (Suzuki et al., 2006), it also requires additional circuits and multiple supply voltages. Then, in order to assist specially the '1'-write operation, we compensate the deteriorated write margins by adopting look ahead dynamic V_{th} control on PD-SOI for 7T SRAM cells with improved read margins. Here, our proposed approach employs only word / bit line signals for the body-biasing control, and therefore any additional signal is not required.

SOI 7T-SRAM WITH LOOK AHEAD BODY BIASING WITH WORD/ BIT LINE SIGNALS

In the proposed 7T-SRAM cell shown in Figure 2, the write bit line (WBL) provides the body-bias for INV(R) and the write and read word lines (WWL and RWL) control the body of access transistors (N3, N4) and driver transistor (N5). Here, the body voltages of nMOS and nMOS in INV (L) are fixed to V_{DD} and GND, respectively, which corresponds to the zero body-bias. In the case of '0'-write (write0) operation, the Vth of pMOS (P1) in INV(R) is lowered by forward body-bias under the condition of WBL = "Low", which accelerates the charging speed of node V_2. In addition, during the '1'-write (write1) operation where the WBL = "High", the Vth of nMOS (N1) can be lowered, hence the discharge current from node V_2 is increased. Namely, the V_{th} of pMOS and nMOS in INV(R) can

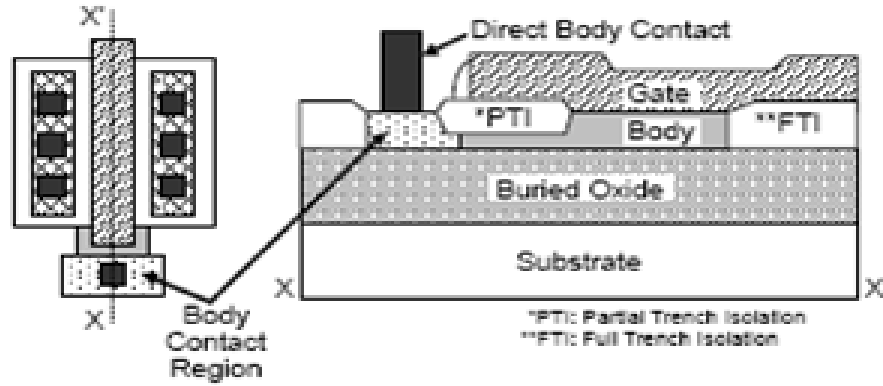*Corresponding author. E-mail: vlsi.shyam@gmail.com Tel: +91-9425146040. Fax: +91-0751-2432988

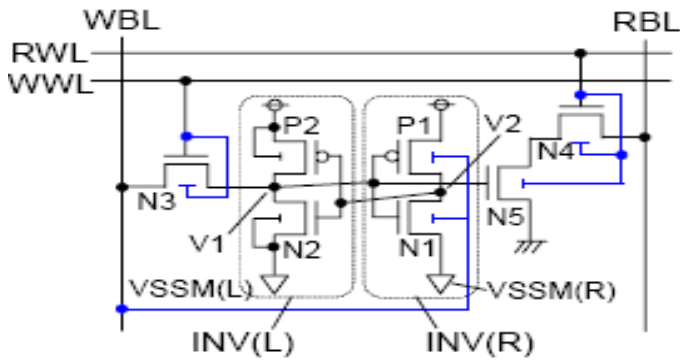**Figure 1.** Schematic diagram of ABC-SOI MOSFET.

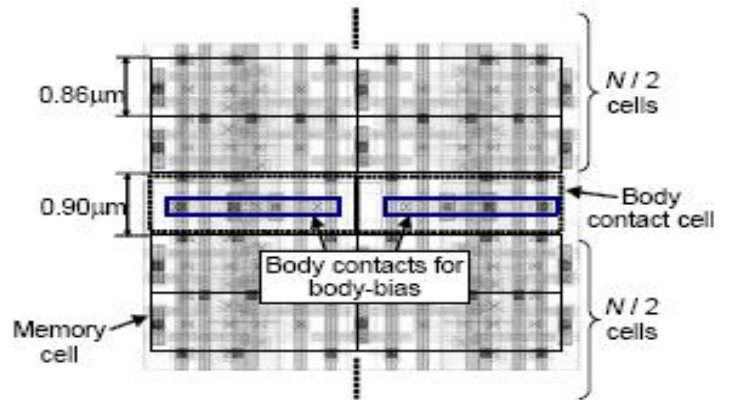**Figure 2.** SOI-7T-SRAM cell adopting look ahead body biasing with word and bit line.

Figure 3. Layout of SOI 7T-SRAM memory cell.

Figure 4. Memory array with body contact cell.
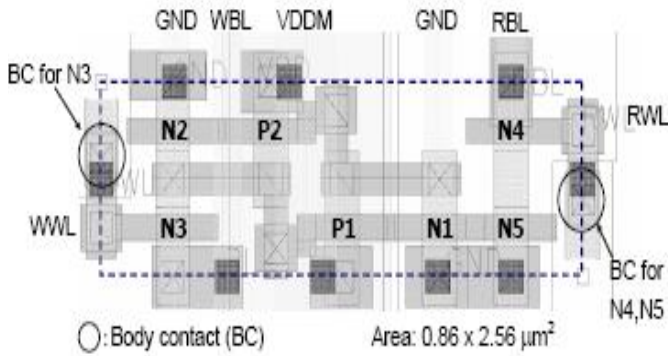
be controlled by the write data of WBL beforehand in order to assist the write operation. Moreover, the body-biases employing the WWL and RWL improves the write and read current owing to the lowered Vth of access transistors (N3, N4) and driver transistor (N5), which therefore shortens the access time both in the write and read operation. Here, since the activated WWL would destroy the stored cell data in the unselected column in the write mode the proposed cell should be applied with the approaches where the column is selected per written block such as the divided word line structure (Yoshimoto et al., 2009).

LAYOUT OF MEMORY ARRAY WITH BODY CONTACT CELL

In order to control the body voltage of individual transistor, a body contact providing the body-bias is required. Considering the intolerable area penalty when all the body contacts are embedded in each memory cell, we examine a layout style that places the body contacts in the memory cell while causing no overhead compared to the conventional 7T- SRAM cell, otherwise the body contacts are shared among several memory cells aligned in the same column. Figure 3 shows the proposed cell layout of 7T-SRAM including the body contacts. Figure 4 illustrates the layout of memory array with the body contact cells, where the body-bias is provided to memory cells through the body contact. Here, the area overhead due to the additional shared body contacts can be reduced by increasing the number (N) of memory cells per body contact. However, the number of memory cells sharing one body contact is limited by a constraint due to the relatively high resistance of the body wiring from the body contact to the body of the transistor.

SIMULATION RESULTS

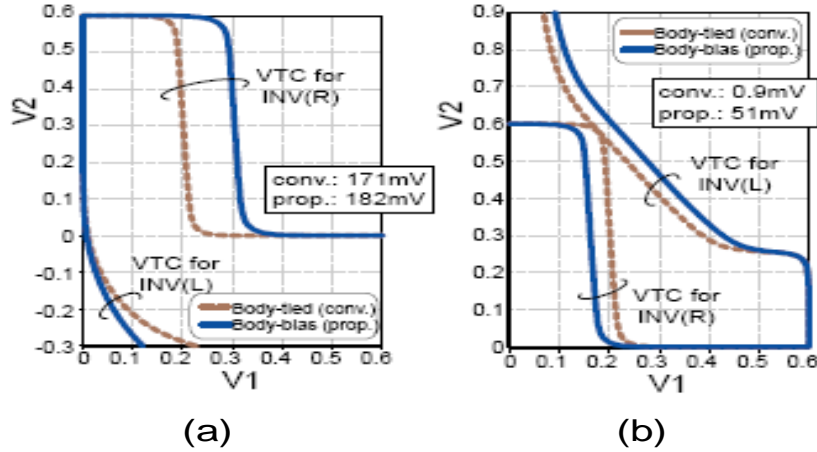SPICE simulation was performed assuming a 90 nm

(a)   **(b)**

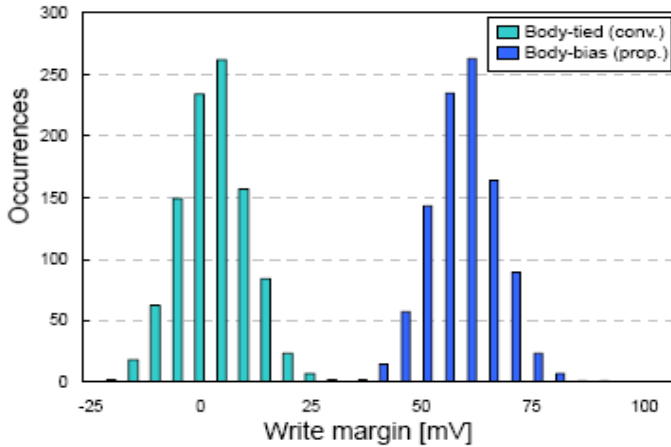**Figure 5.** Improved write margins for proposed Memory Cell (a) '0'-Write Margin (b)'1'-Write.

Figure 6. Impact of global and local Vth variation on the '1'-write margins calculated by the Monte Carlo simulation.

process technology under the conditions that the transistor sizes are L= 0.10 μm, W = 0.16 μm and the supply voltage is set to 0.6 V avoiding the PN leakage current caused by the body-bias. After evaluating the write margins and access time, we have estimated the relation between the number (N) of memory cells sharing one body contact and the area overhead or timing slack of the body voltage which varies due to the resistance and capacitance of body wiring. The threshold voltages are set to $V_{th-n(low)}$ = 0.25 V for the access and driver nMOSs (N1, N3) and $V_{th-n(high)}$ / $V_{th-p(high)}$ = 0.39/-0.44 V for others. Here, the threshold voltages are defined as the gate voltages which make the drain current I_{ds} per width W to be 1 μA/μm when the drain voltage V_{ds} is set to 1.0 V. Body resistances of 119 and 238 k for pMOS and nMOS, respectively, was determined assuming the body contact connects with the neighboring memory cells. The capacitances of word and bit lines for the 256 word × 32

bit memory array are also determined as C_{WL} = 11fF and C_{BL} = 31fF, respectively.

EVALUATION OF WRITE MARGIN

The '0/1 '-write margins for the conventional and proposed 7T-SRAM cells are shown in Figure 5. Here, the conventional cell with the body-tied SOI surely fails in the '1'-write operation due to the lack of write margin. On the other hand, the voltage transfer characteristics (VTCs) for the proposed cell are shifted owing to the body-bias employing the look-ahead control signals of word / bit lines, which expands the write margins to 182 and 51 mV in the '0' and '1' write modes, respectively

IMPACT OF V_{TH} VARIATION OF WRITE MARGIN

The dependence of write margins derived from a variation in the threshold voltage (V_{th}) was analyzed. Figure 6 shows the distribution of the '1'-write margins for a 7T-SRAM cell based on the 1k-point Monte Carlo simulations. Here, the global and local (V_{th}) variations of 3 s are reflected to these histograms, where the standard deviations of (V_{th}) is assumed that 3 s corresponds to 10% of V_{th}.

According to the results, even though the mean of '1'-write margin in the conventional body-tied approach barely becomes a positive value, most memory cells will surely fail in the '1'-write operation due to significant lack of write margin. On the other hand, the mean in the proposed approach has been improved from 0.7 to 50.9 mV, while keeping the standard deviation of write margin as 7.7 mV. Hence, a smaller coefficient of variation (s/μ) of the write margin is expected for the proposed memory cell.
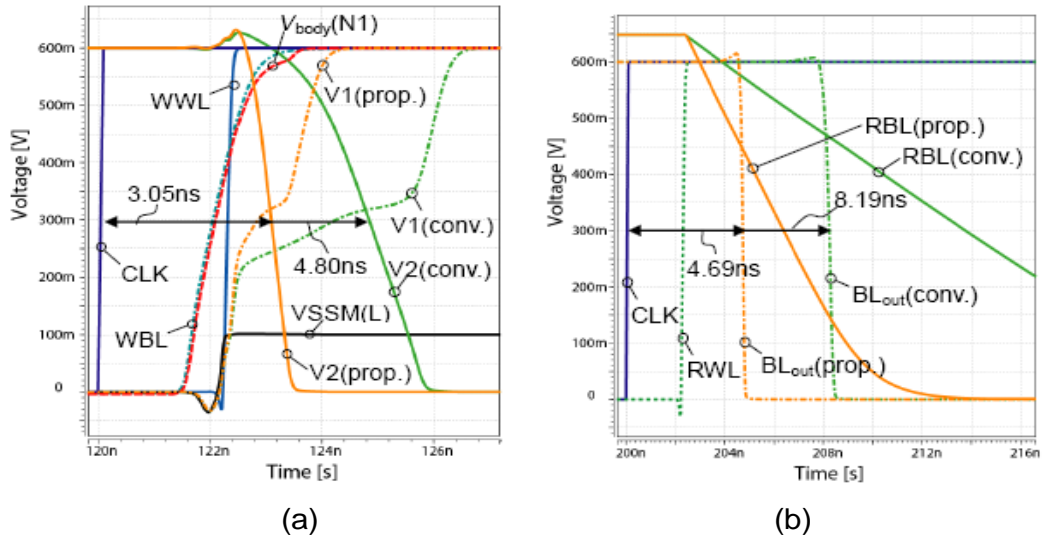
Figure 7. Access time comparison based on simulated waveforms. (a) '1'-Write mode. (b) Read mode.
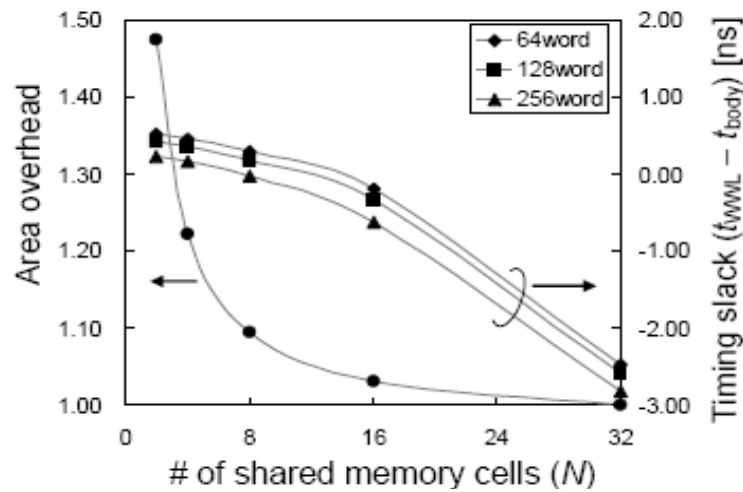

Figure 8. Trade –off between the number (N) of shared memory cells and area overhead /timing slack of body voltage.

EVALUATION OF ACCESS TIME

In Figure 7, the access time when adopting the boosted VSS node (Chang et al., 2005) for the memory cell is shown to ensure the '1'-write operation even in the conventional body-tied approach here, the access time in the '1'-write rather than '0'-write operation becomes critical due to the threshold voltage loss of access transistor (N3). The waveforms shown in (Figure 7) correspond to the clock (CLK), word lines (WWL / RWL), bit lines (WBL / RBL), data retention nodes (V1 / V2), output data signal (BL$_{out}$) and body voltage (V$_{body}$). Here the access time is defined as the period from the point of V$_{DD}$ /2 in CLK during the low to high transition to that in the data retention node V2 or output data signal (BL$_{out}$) during the

data inverting operation. The body-bias improves the charge and discharge current at the data nodes V1 and V2, and hence shortens the access time by 36 and 43% in the '1'-write and read mode, respectively.

DISCUSSION ON AREA OVERHEAD AND TIMING SLACK OF BODY VOLTAGE

Here, we discuss the trade-off relation between the area overhead and timing slack of the body voltage for the number (N) of the memory cells sharing one body contact. In Figure 8, the area overheads are normalized to the conventional layout style where a body contact is shared by 32 memory cells. Regarding the body wiring, the body

resistances for pMOS and nMOS were estimated as 111, 222 k/μm, respectively, and the body capacitance of 0.0432 fF/μm. Also, the timing slack of the body voltage at the farthest memory cell from the body contact was then evaluated. For the write buffer driving the body voltages and bit lines, the size is decided $W_{buf} = 2.5$ μm which is optimized in terms of the energy-delay product.

According to the results for N from 2 to 32, the timing slack which represents the period from the $V_{DD}/2$ in body voltage to that in WWL ($t_{WWL} - t_{body}$) decreases with N. In that case of memory with 256-word, even though the timing slack of the body voltage is 0.23 ns when N = 2, the value is deteriorated to -2.82 ns when N = 32. Here the maximum number (N_{max}) of sharing memory cells should be decided within the limit of controlling the body voltage perfectly before the write operation in the memory cell. The timing slack in the simulation results constrains an upper limit of $N_{max} = 8$ which barely satisfies "$t_{WWL} - t_{body} > 0$" and hence ensure the expanded write margins before the write operation. The area overhead is 10% when $N_{max} = 8$. Moreover, even though the ideal condition of "$t_{WWL} - t_{body} > 0$" is not satisfied, we still expect the access time reduction as long as the timing slack meets "$t_{WWL} - t_{body} > -2.53$ ns" according to the write period of 2.53 ns from WWL to the data node V2 in the conventional approach shown in Figure 7(a).

Conclusion

Although a 7T-SRAM with an area-tolerable separated read port improves read margins and therefore seems one of the candidates in deep sub-100 nm era, it still has a difficulty of deteriorated write margins. We then have proposed a memory cell adopting a look-ahead body-bias which dynamically controls the threshold voltage in order to assist the write operation. Simulation results have shown improvement in both the write margins and access time.

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