International Journal of the Physical Sciences Vol. 6(30), pp. 7026 - 7034, 23 November, 2011
Available online at http://www.academicjournals.org/IJPS
DOI: 10.5897/IJPS11.401
ISSN 1992 - 1950 ©2011 Academic Journals

Full Length Research Paper

Optimization of input process parameters variation on threshold voltage in 45 nm NMOS device

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Accepted 19 October, 2011

In this study, Taguchi method was used to optimize the influence of process parameter variations on threshold voltage (V_{TH}) in 45 nm n-channel metal oxide semiconductor (NMOS) device. The orthogonal array, the signal-to-noise ratio, and analysis of variance were employed to study the performance characteristics of a device. In this paper, eleven process parameters (control factors) were varied for 2 levels to perform 12 experiments. Whereas, the two noise factors were varied for 2 levels to get four readings of V_{TH} for every row of experiment. V_{TH} results were used as the evaluation variable. This work was done using technology computer-aided design (TCAD) simulator, consisting of a process simulator, ATHENA and device simulator, ATLAS. These two simulators were combined with Taguchi method to aid in design and optimize the process parameters. In this research, compensation implantation energy was identified as one of the process parameters that have the strongest effect on the response characteristics. While the halo implantation dosage was identified as an adjustment factor to get the nominal values of threshold voltage for NMOS device equal to 0.176 V.

Key words: Process simulation, device simulation, control factor, analysis of variance, Taguchi method.

INTRODUCTION

For more than 30 years, the metal oxide semiconductor field effect transistor (MOSFET) have continually been scale down in size and in channel length from micrometers to sub-micrometers and then to sub-micrometers range following Moore's Law. The channel length MOSFET is reduced from 100 to 45 nm. The size reduction of the device makes great improvement to MOSFET operation (Taur et al., 1995). Present day metal-oxide semiconductor (MOS) process invariability uses ion implantation into the channel region, which alters the doping profile near the surface of silicon substrate (Kang and Leblebici, 2003). The ion implantation process provides much more precise control of doping than the diffusion process (Ninomiya et al., 2009). For example, the dopant concentration and junction depth cannot be independently controlled in the diffusion process because both are related to the diffusion temperature and time; ion implantation can independently control both dopant concentration and junction depth.

Dopant concentration can be controlled by the combination of ion beam current and implantation time, whereas junction depth can be controlled by the ion energy. By changing dose, energy and rotation of these implants can change the profile and the electrical characteristics of the MOSFET device (Ninomiya et al., 2009; Wang et al., 2005). One of the most important physical parameters for MOSFET is its threshold voltage (V_{TH}). V_{TH} is the minimum gate voltage needed to create a channel between source and drain. It can be defined as the minimum voltage for strong inversion to occur (Croon et al., 2002). Many researchers have proposed method not only to control the electrical characteristics, mainly threshold voltage and saturation current but also to optimize the process parameters' variation. In design of devices with deep sub micron technologies, the analysis of variability has become a very important tool, to predict

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the response variation very early in the design cycle due to process parameter spreads (Nassif et al., 1984). The variations will impact the performance of device, which may exhibit wider variability leading to the degradation of yield in modern technologies and applications (Sylvester et al., 2008).

In this paper, for identifying semiconductor process parameters, whose variability would impact most on the device characteristics, is realized using Taguchi method. Taguchi method has become a powerful tool for improving productivity during research and development (Phadke, 1998). This is because the Taguchi method is a systematic application of design and analysis of experiments for the purpose of designing and improving product quality at the design stage. A large number of experiments have to be carried out when the number of the process parameters increases. To solve this task, the Taguchi method uses a special design of orthogonal arrays to study the entire process parameter space with only a small number of experiments (Esme, 2009; Sharma et al., 2005). In the current study (Nalbant et al., 2007), for the design of the experiment with a mixed matrix of 11 process parameters with 2 levels and 2 noise factors with 2 levels, there will be as many as 324 (2^{11}×2^2) runs of testing if using the conventional full factorial design. The testing of only 48 runs with the Taguchi method greatly reduces the number of tests and increases the efficiency. Using an orthogonal array to design the experiment could help the designers to study the influence of multiple controllable factors on the average of quality characteristics and the variations in a fast and economic way, while using a signal-to-noise ratio to analyze the experimental data could help the designers of the product or the manufacturer to easily find out the optimal parametric combinations (Syros, 2003; Naidu, 2008).

MATERIALS AND METHODS

P-type silicon with <100> orientation is used as the main substrate for this experiment. A 200Å oxide layer was grown on the top of the silicon bulk. This oxide layer is used as the mask for P-well implantation process. Then, the oxide layer was etched after the doping process was completed. It was followed by annealing process to strengthen the structure. Next, Shallow Trench Isolation (STI) was developed to isolate neighbouring transistor. A 130 Å stress buffer was grown on the wafers with 25 min diffusion processes. Then, a 1500 Å nitride layer was deposited using the Low Pressure Chemical Vapour Deposition (LPCVD) process. This thin nitride layer was acted as the mask when silicon was etched to expose the STI area. Photo resistor layer was then deposited on the wafers, and unnecessary part will be etched using the Reactive Ion Etching (RIE) process. An oxide layer was grown on the trench sides to eliminate any impurity from entering the silicon substrate. Chemical Mechanical polishing (CMP) was then applied to eliminate extra oxide on the wafers. Lastly, STI was annealed for 15 min at 900℃ temperature. A sacrificial oxide layer was then g rown and etched to eliminate defects on the surface. The gate oxide was grown and a Boron Difluoride (BF_2) threshold-adjustment implant was done in the channel region through this oxide. The polysilicon gate was then deposited and defined followed by the halo implantation.

In order to get an optimum performance for NMOS device, indium was doped. Halo implantation was followed by depositing sidewall spacers. Sidewall spacers were then used as a mask for source/drain implantation. Arsenic atom was implanted at a desired concentration to ensure the smooth current flow in NMOS device. Silicide layer was formed and then annealed on the top of polysilicon. The next step in this process was deposited of Boron Phosphor Silicate Glass (BPSG) layer. This layer will be acted as Premetal Dielectric (PMD), which is the first layer deposited on the wafer surface when a transistor was produced. This transistor was then connected with aluminum metal. After this process, the second aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts (Elgomati and Ahmad, 2007; Elgomati et al., 2011). The procedure was completed after the metallization and etching were performed for the electrode formation, and the bonding pads were opened. Once the devices were built with ATHENA, the complete devices can be simulated in ATLAS to provide specific characteristics such as the I_D versus V_{GS} curve. The threshold voltage (V_{TH}) can be extracted from that curve (Goel et al., 1995).

Taguchi orthogonal L_{12} array method

The optimizations of the NMOS device have been done by changing individual process parameters (control factors) laid out by the ATHENA (Goel et al., 1995). The factors that were modified and examined include: The substrate implant dose, halo implant tilt angle, gate-oxide diffusion temperature, threshold voltage (V_{TH}) implant dose, V_{TH} implant energy, halo implant dose, halo implant energy, Source/Drain (S/D) implant dose, S/D implant energy, compensation implant dose and compensation implant energy. Whereas, the two noise factors are sacrificial oxide temperature and annealing process temperature. These noise factors were varied for 2 levels to get four readings of V_{TH} for every row of experiment. The values of the process parameter and noise factor at the different levels are listed in Tables 1 and 2, respectively.

In this research, an $L_{12}(2^{11})$ orthogonal array which has 12 experiments was used. The experimental layout for the process parameters using the $L_{12}(2^{11})$ orthogonal array is shown in Table 3.

RESULTS AND DISCUSSION

The electrical characteristics result of the first set of experiment that has been done by using ATLAS module was discussed. Beside that, optimization result of NMOS device by using Taguchi method approach is also shown here.

Analysis of 45 nm NMOS device

Figure 1 show clearly on the doping concentration across the 45 nm NMOS transistor. The figure shows the tabulation of silicon, silicon dioxide, polysilicon, silicon nitride, cobalt salicide and aluminum. Doping concentration is one of the factors that will determine the electrical characterization of the transistor. A good doping concentration will ensure the transistor works well with clear enhance gate control and fewer leakage current (Goel et al., 1995).

Figure 2 shows the graph of drain current (I_D) versus gate

Table 1. Process parameters and their levels.

Symbol	Process parameter	Unit	Level 1	Level 2
A	Substrate Implant Dose	atom cm^{-3}	3.70E12	3.73E12
B	Pocket-Halo Implant Tilt Angle	Degree	20	23
C	Gate-Oxide Diffusion Temperature	℃	825	823
D	V_{TH} Implant Dose	atom cm^{-3}	1.70E11	1.72E11
E	V_{TH} Implant Energy	keV	5	6
F	Pocket-Halo Implant Dose	atom/cm^3	3.25E13	3.30E13
G	Pocket-Halo Implant Energy	keV	180	170
H	S/D Implant Dose	atom cm^{-3}	5.80E13	5.85E13
I	S/D Implant Energy	keV	15	16
J	Compensation Implant Dose	atom cm^{-3}	3.70E13	3.80E13
K	Compensation Implant Energy	keV	60	65

Table 2. Noise factors and their levels.

Symbol	Noise factor	Unit	Level 1	Level 2
N	Sacrificial oxide temperature	℃	950 (N_1)	951 (N_2)
M	Annealing process temperature	℃	910 (M_1)	915 (M_2)

Table 3. Experimental layout using L_{12} (2^{11}) orthogonal array.

Experiment no.	Process parameter level										
	A	B	C	D	E	F	G	H	I	J	K
1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	1	1	1	2	2	2	2	2	1
3	1	1	2	2	2	1	1	1	2	2	2
4	1	2	1	2	2	1	2	2	1	1	2
5	1	2	2	1	2	2	1	2	1	2	1
6	1	2	2	2	1	2	2	1	2	1	2
7	2	1	2	2	1	1	2	2	1	2	2
8	2	1	2	1	2	2	2	1	1	1	1
9	2	1	1	2	2	2	1	2	2	1	2
10	2	2	2	1	1	1	1	2	2	1	1
11	2	2	1	2	1	2	1	1	1	2	2
12	2	2	1	1	2	1	2	1	2	2	1

gate voltage (V_G) at drain voltage, V_D = 0.05 V and V_D = 1.1 V for NMOS device (Chen et al., 2004). The nominal value of threshold voltage for this device is 0.175 V (ITRS, 2008).

The results of V_{TH} were analyzed and processed with Taguchi method to get the optimal design. The optimized results from Taguchi method were simulated in order to verify the predicted optimal design.

Analysis of input process parameters influence on threshold voltage

Twelve different experiments in NMOS device was performed using the design parameter combinations in the specified orthogonal array table. Four specimens were simulated for each of the parameter combinations. The completed response for V_{TH} data is shown in Table 4.

After twelve experiments of L_{12} array have been done, the next step was to determine, which control factors gave more effect to a device characteristics. Signal-to-noise (S/N) ratio was used to easily find out the optimal process parameters and analyze the experimental data. There are three categories of the performance characteristics in the analysis of the S/N ratio, that is, the lower-the-better, the higher-the-better, and the nominal- the-better (Syros, 2003). The S/N ratio for each level of process parameters is computed based on the S/N analysis.

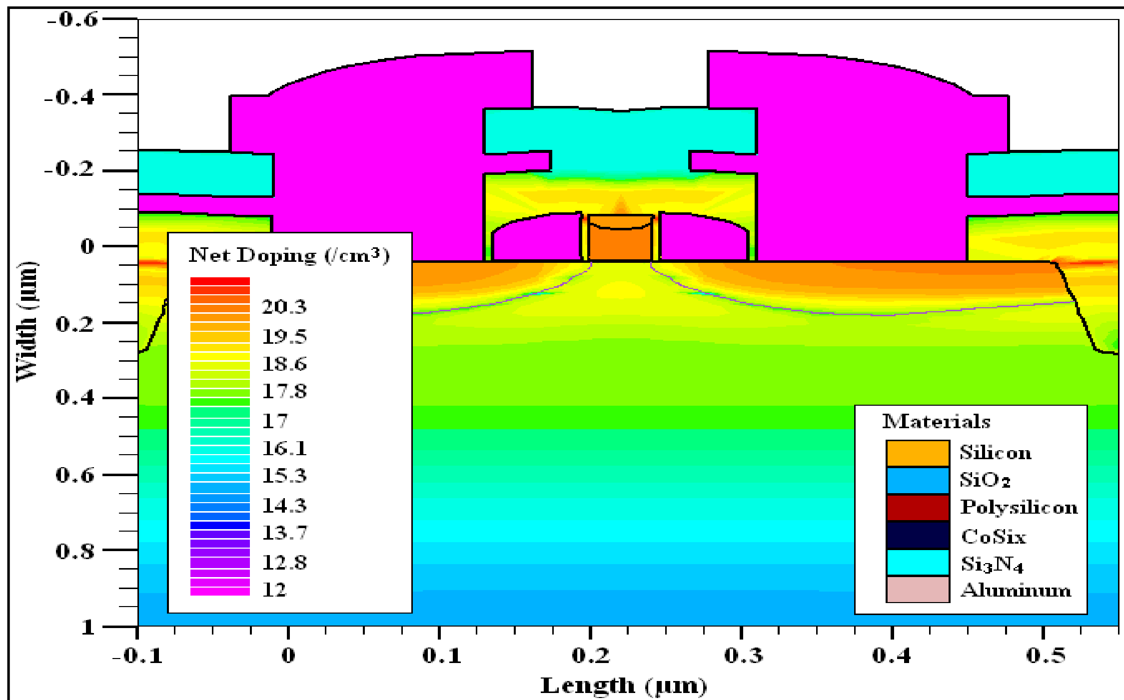

Figure 1. 45 nm NMOS transistor doping concentration.

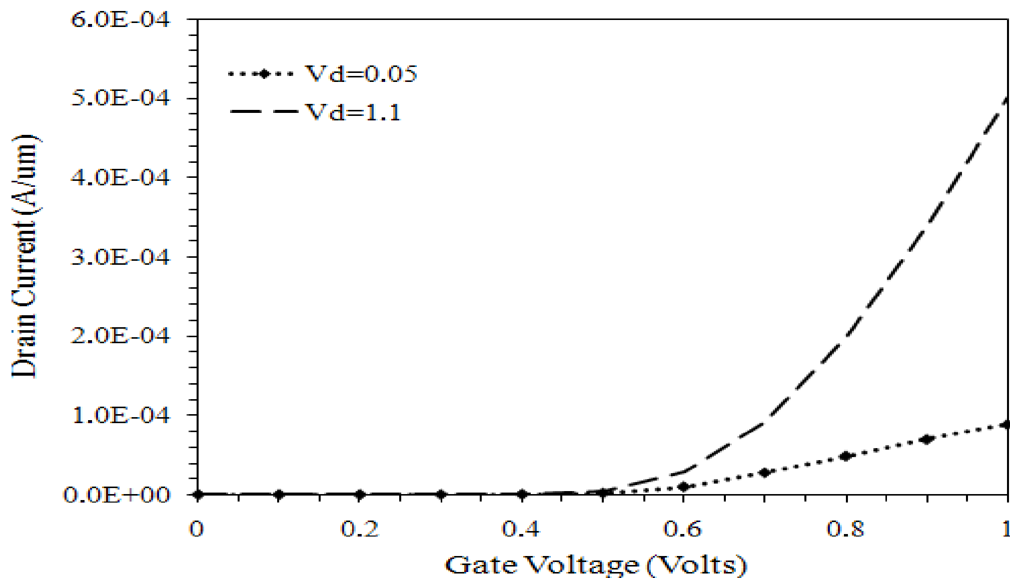

Figure 2. Graph I_D-V_G for 45 nm NMOS device.

Regardless of the category of the performance characteristic, the larger S/N ratio corresponds to the better performance characteristic. Therefore, the optimal level of the process parameters is the level with the highest S/N ratio (Abdullah et al., 2009; Naidu, 2008).

In this research, threshold voltage of the 45 nm device belongs to the nominal-the-best quality characteristics. This S/N Ratio is selected to get threshold voltage value closer or equal to a given target value (0.175 V), which is also known as nominal value (Naidu, 2008). The S/N

Table 4. V_{TH} values For NMOS device.

Experiment no.	Threshold voltage (Vth)			
	Vth1	Vth2	Vth3	Vth4
1	0.1394	0.1322	0.1389	0.1327
2	0.1621	0.1634	0.1616	0.1639
3	0.1608	0.1491	0.1603	0.1496
4	0.1685	0.1679	0.1681	0.1684
5	0.1391	0.1375	0.1386	0.1380
6	0.1192	0.1584	0.1187	0.1590
7	0.1242	0.1369	0.1237	0.1375
8	0.2069	0.2048	0.2064	0.2053
9	0.1426	0.1324	0.1421	0.1329
10	0.1301	0.1342	0.1296	0.1347
11	0.1745	0.1777	0.1740	0.1782
12	0.1365	0.1188	0.1360	0.1193

Table 5. Mean, variance and S/N ratios for NMOS device.

Experiment no.	Mean	Variance	S/N ratio (Mean)	S/N ratio (Nominal-the-Best)
1	0.136	1.50E-05	-17.34	30.88
2	0.163	1.16E-06	-15.77	43.57
3	0.155	4.19E-05	-16.20	27.58
4	0.168	7.67E-08	-15.48	55.67
5	0.138	4.87E-07	-17.18	45.94
6	0.139	5.27E-04	-17.15	15.63
7	0.131	5.86E-05	-17.68	24.64
8	0.206	9.37E-07	-13.73	46.56
9	0.138	3.14E-05	-17.23	27.79
10	0.132	7.14E-06	-17.58	33.89
11	0.176	4.65E-06	-15.08	38.24
12	0.128	9.87E-05	-17.88	22.18

ratio (Nominal-the-best), η can be expressed as $\eta = 10\,\mathrm{Log}_{10}\left[\frac{\mu^2}{\sigma^2}\right]$ (Phadke, 1998), whereas $\mu = \frac{Y_i + ... + Y_n}{n}$ and $\sigma^2 = \frac{\sum_{i=1}^{n}(Y_i - \mu)^2}{n-1}$. While n is number of tests and Y_i the experimental value of the threshold voltage, μ is mean and σ is variance. In the nominal-the-best, there are two types of factor to find which are dominant and adjustment factors. The S/N ratios (Nominal-the-best) for the device were calculated and are given in Table 5 (Phadke, 1998). The effect of each process parameter on the S/N ratio at different levels can be separated out because the experimental design is orthogonal. The S/N ratio (SNR) for each level of the process parameters is summarized in Table 6. In addition, the overall mean SNR for the nine experiments is also calculated.

Figures 3 and 4 show the S/N ratio and means graphs respectively for NMOS device. Basically, the larger the S/N ratio, the quality characteristic for the threshold voltage is better (Esme, 2009). The closer the quality characteristic value to the target, the better the product quality will be (Naidu, 2008).

Analysis of variance (ANOVA)

The analysis of variance (ANOVA) is a common statistical technique to investigate which of the process parameters significantly affect the performance character-

Table 6. S/N responses for the threshold voltage.

Symbol	Process parameter	S/N ratio (nominal-the-best)		Max - Min
		Level 1	Level 2	
A	Substrate implant dose	36.55	32.21	4.34
B	Pocket-halo implant tilt angle	33.50	35.26	1.76
C	Gate-oxide diffusion temperature	36.39	32.37	4.02
D	Vth implant dose	37.17	31.59	5.58
E	Vth implant energy	31.14	37.62	6.48
F	Pocket-halo implant dose	32.47	36.29	3.82
G	Pocket-halo implant energy	34.06	34.71	0.65
H	S/D implant dose	30.18	38.58	8.40
I	S/D implant energy	40.32	28.44	11.88
J	Compensation implant dose	35.07	33.69	1.38
K	Compensation implant energy	27.84	40.92	13.08

Overall mean of SNR = 34.31 dB.

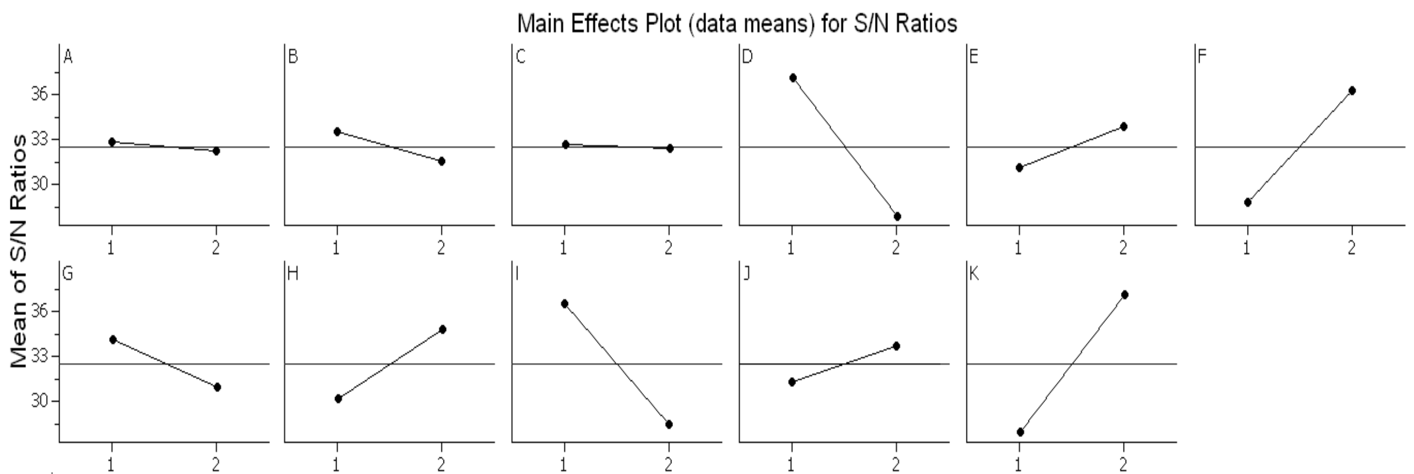

Figure 3. S/N ratio graph for threshold voltage in NMOS device.

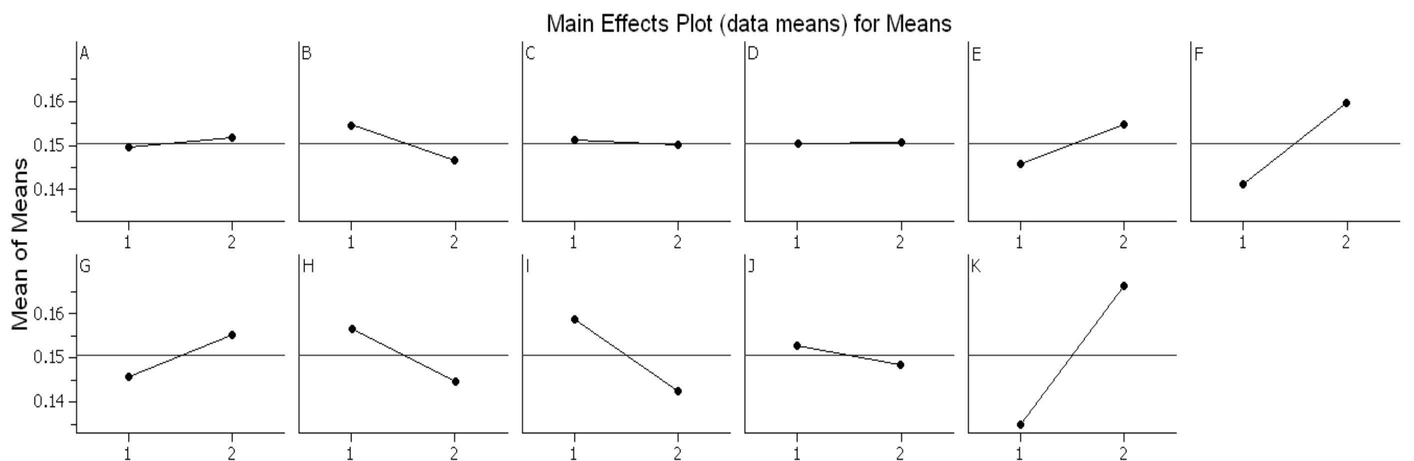

Figure 4. Means graph for threshold voltage in NMOS device.

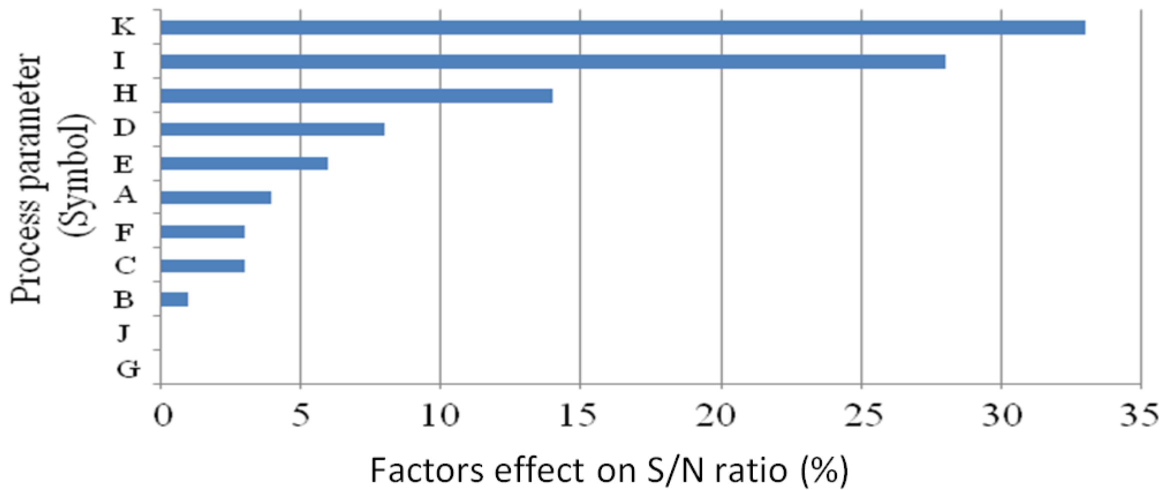

Figure 5. Pareto plot of V_{TH} for NMOS device.

characteristics (Yang et al., 2007). It calculates parameters known as sum of squares (SS), degree of freedom (DF), variance, F-value and percentage of each factor. The variance (mean square) of the process parameter tested is $V = \frac{SS}{DF}$ (Phadke, 1998). F-value for each process parameter is the ratio of variance due to the effect of a factor and variance due to the error term. It is used to measure the significance of the factor under investigation with respect to the variance of all the factors included in the error term. When the variance of the error is zero, the F-value for factors A, B, C, D, E, F, G, H, I, J and K is undetermined. Then the variance of the error can be combined with another smaller factor variance to calculate a new error variance which can be used to produce meaningful results. The process of disregarding an individual factor's contribution and then subsequently adjusting the contribution of the other factor is known as pooling.

The results of ANOVA for the NMOS device are shown in Table 7. According to these analyses, the most dominant factors for S/N ratio are factor K (Compensation implant energy – 33%) and factor I (S/D implant energy – 28%). Therefore, these factors should be set at 'best setting' and cannot be used as an adjustment factors. Whereas, factor F (Pocket-halo implant dose) was described as an adjustment factor because it has the large effect on mean (16.78%) and small effect on variance (3%) if compared with other factors. The percent factor effect on S/N ratio indicates the priority of a factor (process parameter) to reduce variation. For a factor with a high percent contribution and a small variance (mean square) will have a great influence on the performance (Nalbant et al., 2007).

The Pareto plots of standardized effect of V_{TH} for 45 nm NMOS device are presented in Figure 5. The Pareto plot compares the relative magnitude and the statistical significance of all the main effects (process parameters) and ranks the parameters accordingly. The effective plots are in the decreasing order of the absolute value of the effects. From Figure 5, it can be seen that for the response, V_{TH}, K (Compress implant energy-33%), I (S/D implant energy-28%), H (S/D implant dose-14%), D (Vth implant dose-8%) and E (Vth implant energy-6%) are the top five significant parameters.

The analysis of average performance showed that the optimum condition is A_1, C_1, D_1, E_2, F_2,H_2, I_1, K_2. Because factor B (Pocket-halo implant tilt angle), factor G (Pocket-halo implant energy) and factor J (Compensation implant dose) were found to be non significant (pooled) in threshold voltage, they could be set at any level (Phadke, 1998). The full recommendation for optimization is A_1, B_2, C_1, D_1, E_2, F_2, G_2, H_2, I_1, J_1, K_2.

Confirmation test

The confirmation experiment is the final step in the first interaction of the design of the experiment process. The purpose of the confirmation experiment is to validate the conclusions drawn during the analysis phase (Esme, 2009). Best setting of the process parameters for NMOS device that had effects on V_{TH}, which had been suggested by Taguchi method is shown in Table 8.

Once the optimal level of the process parameters is selected, the final simulation was performed to verify the accuracy of the Taguchi method prediction. The results of the final simulation for V_{TH} is shown in Table 9. Before the optimization approaches, the best S/N ratio (Nominal-the-best) is 55.67 dB at row of experiment no. 4 (Table 5). Whereas the variance is 7.67×10^{-8} V and mean for

Table 7. Results of ANOVA for NMOS device.

Symbol	Process parameter	DF	Sum of square	Mean square	F-Value	Factor effect on SNR (%)	Factor effect on mean (%)
A	Substrate implant dose	1	56	56	368	4	0
B	Pocket-halo implant tilt angle	1	9	9	60	1	2.69
C	Gate-oxide diffusion temperature	1	48	48	316	3	0.25
D	Vth implant dose	1	93	93	609	6	0.20
E	Vth implant energy	1	126	126	821	8	3.92
F	Pocket-halo implant dose	1	44	44	285	3	16.78
G	Pocket-halo implant energy	1	0	0	8	0	3.98
H	S/D implant dose	1	212	212	1383	14	5.85
I	S/D implant energy	1	424	424	2764	28	13.07
J	Compensation implant dose	1	6	6	37	0	0.76
K	Compensation implant energy	1	513	513	3347	33	52.51

[a]At least 95% confidence.

Table 8. Results of the confirmation experiment.

Symbol	Process parameter	Unit	Best value
A	Substrate implant dose	atom/cm^3	3.70E12
B	Pocket-halo implant tilt angle	Degree	23
C	Gate-oxide diffusion temperature	^{o}C	825
D	Vth implant dose	atom/cm^3	1.70E11
E	Vth implant energy	keV	6
F	Pocket-halo implant dose (as an adjustment factor)	atom/cm^3	3.30E13
G	Pocket-halo implant energy	keV	170
H	S/D implant dose	atom/cm^3	5.85E14
I	S/D implant energy	keV	15
J	Compress implant dose	atom/cm^3	3.70E13
K	Compress implant energy	keV	65

Table 9. Results of the confirmation experiment for threshold voltage.

Threshold voltage (Volts)				S/N ratio (Mean)	S/N ratio (nominal-the-best)
Vth1	Vth2	Vth3	Vth4		
0.1754	0.1757	0.1753	0.1756	-15.11 dB	59.66 dB

threshold voltage is 0.168 V. The percentage difference of this threshold voltage value from the nominal value, 0.175 V (ITRS, 2008) is 4%.

After the optimization approaches, the S/N ratio (Nominal-the-best) and S/N Ratio (Mean) of threshold voltage for NMOS device are 59.66 and -15.11 dB, respectively. These values are within the predicted range. For S/N ratio (Nominal-the-best), 59.66 dB is within predicted range S/N ratio of 69.08 to 57.26 dB (63.2 ± 5.91 dB). While for S/N ratio (Mean), -15.11 dB is within predicted range S/N ratio of -14.15 to -15.27 dB (-14.7 ± 0.56 dB). These show that Taguchi method can predict the optimum solution in finding the 45 nm NMOS fabrication recipe with appropriate threshold voltage value.

The variance and threshold voltage for the device after optimization approaches are 3.33×10^{-8} and 0.176 V respectively at t_{ox}=1.06 nm. The results show that the variance is slight decrease and threshold voltage value is closer to the nominal value (target). The V_{TH} value is just 0.57% different from the target. This value is exactly same with International Technology Roadmap for Semi-conductor (ITRS) prediction (ITRS, 2008). The closer the quality characteristic value to the target, the better the

product quality will be (Nalbant et al., 2007). At row of experiment no. 11, the mean for threshold voltage is 0.176 V. It is exactly same with the target but the variance is high (4.65×10^{-6} V) and S/N ratio is small (38.24 dB). The S/N ratio value is also not within predicted range S/N ratio of 69.08 to 57.26 dB.

Conclusion

In conclusion, the optimum solution in achieving the desired transistor was successfully predicted by using Taguchi method. There are many physical limitations involved as the size gets smaller, approaching the molecular or atomic limitations of the substrate and dopant. Threshold voltage (V_{TH}) is the main response studied in this project as it is the main factor in determining whether digital device works or not. Taguchi method design is used to develop a systematic design of experiment. It has many variants that can be applied to modeling device and a lot of process parameter can be used. Taguchi method already has been applied to get a robust and better design. The level of importance process parameters on the threshold voltage is determined by using ANOVA. Based on the ANOVA method, the highly effective parameters on threshold voltage were found as compensation implant dose (33%) and S/D implant energy (28%), whereas halo implant dose was described as an adjustment factor.

ACKNOWLEDGEMENTS

The authors would like to thank the Ministry of Higher Education (MOHE) for their financial support as well as Photonic Lab Universiti Kebangsaan Malaysia (UKM) and Universiti Teknikal Malaysia Melaka (UTeM) for moral support throughout the project.

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