International Journal of the Physical Sciences Vol. 6(5), pp. 1146-1151, 4 March, 2011
Available online at http://www.academicjournals.org/IJPS
DOI: 10.5897/IJPS10.453
ISSN 1992 - 1950 © 2011 Academic Journals

Full Length Research Paper

Double-gate tunnel FET with silicon nitride and oxynitride

A. Bahari[1]*, F. Pourzaman[2] and M. Hoseni[2]

[1]Department of Physics, University of Mazandaran, Babolsar, Iran.
[2]Department of physics, Islamic Azad University, Tehran-center branch, Tehran, Iran.

Accepted 27 January 2011

To extend the scaling limit of thermal SiO_2 in the ultrathin regime when the direct tunneling and leakage current becomes significant, we study the properties of silicon nitride and silicon oxynitride gate dielectrics as good candidates for the next nano transistor devices. In this paper, high-quality silicon nitride (and/or oxynitride) films made by chemical vapor deposition (CVD) technique are described. The experimental and theoretical works based on ZAF (Z: Atomic number, A: Absorption and F: Fullerence) and Landaur-Buttiker (LB) methods, respectively, make silicon nitride (or oxynitride) an attractive candidate to succeed thermal SiO_2 as an advanced gate dielectric in future generations of ULSI devices.

Key words: Nano transistor, thin film, gate dielectric and silicon nitride.

INTRODUCTION

An integrated circuit is provided including an field-effect-transistor (FET) gate structure formed on a silicon substrate. In the current metal-oxide-semiconductor-field-effect-transistor (MOSFET), it includes SiO_2 film as a gate dielectric on the Si(100) substrate, and a metal or polysilicon layer overlying the gate dielectric and in contact therewith.

As MOSFETs continue to get smaller and run into fundamental performance limitations, there is a renewed interest in exploring devices that use tunneling for their ON-current (Boucart and Ionescu, 2005; Bahari et al., 2005; Daggubati et al., 2009; Bahari et al., 2006; Zhao et al., 2009; Morgen et al., 2007; Bahari et al., 2008; Hobbs et al., 2002; Bahari and Riazian, 2009; Bahari et al., 2009).

Some researchers believe that Carbon nano tube field effect transistor (CNTFET) can be used in stead of MOSFET. However, we have considered single walled (SW) CNT as a channel and silicon nitride and silicon oxynitride as gate dielectrics (DGD) for future nano transistor devices (Bahari et al., 2005; Daggubati et al., 2009; Hobbs et al., 2002).

Recently Bahari et al. (2009), have studied analytically the effect of double-gate dielectric (DGD) instead of single-gate dielectric and found that DGD can significantly reduce leakage and tunneling current. Theses gate dielectrics are grown on the silicon substrate and studied with using Auger electron spectroscopy (AES), Sputtering and energy dispersive x – ray (EDX) techniques. These issues indicate that we have to search for the other gate dielectric to fill this gap. The high dielectric constant (HK) materials, here, Si_3N_4 (K = 7.8) and/or SiO_xN_y can be considered for the sub-65 nm MOS structure because the conventional SiO_2, as stated previously, is too thin (for example, 2 nm) to minimize the leakage, tunneling current and the out diffusion of boron from the gate. A thick layer can be required with the high-k material to lower the parasitic capacitance. Many issues have to be solved before it is acceptable for the products. In this work, silicon nitride (as well as silicon oxynitride) as a type of high-k dielectric is studied to prevent the top-to-bottom metal shortage, which is a killing factor for the

*Corresponding author. E-mail: alibahari@ymail.com.

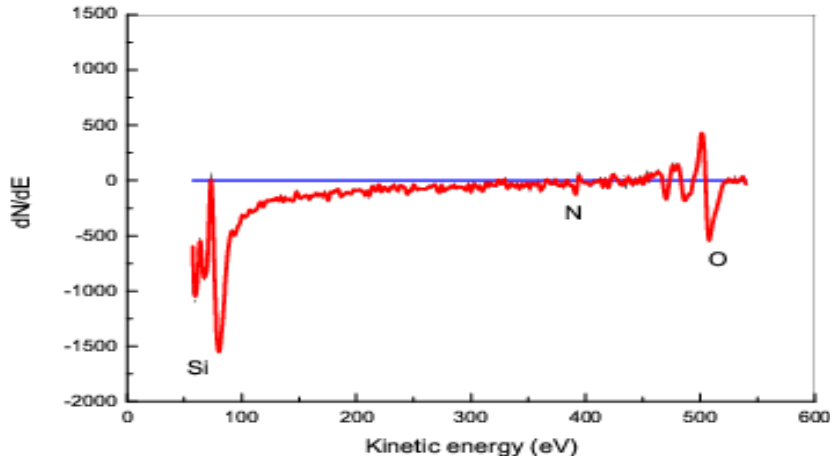

Figure 1. AES spectrum of silicon nitride.

yield.

The high-k dielectric ($Si_3 N_4$ and SiO_xN_y) material is usually used in combination with a high quality dielectric interface layer to lower the interface density of states. Numerous attempts to develop the CVD silicon nitride into a viable gate dielectric directly for CMOS have encountered two major difficulties: (1) poor nitride/Si interface properties and (2) high density of bulk traps in silicon nitride. The first difficulty does not apply to CNTFETs in that only the CNTs would be in direct contact with silicon nitride, and it is expected that the fully bonded CNT (with no dangling bonds) would not give rise to $Si_3 N_4$ and SiO_xN_y /CNT interface states.

The second drawback is for more complicated but should be solvable as emerging thin film CVD technique. For this purpose, DG tunnel FET devices, using $Si_3 N_4$ and SiO_xN_y, have been studied to find if it can exhibit very strong resistance to boron penetration and leakage /tunneling currents.

EXPERIMENTAL PROCEDURES AND DISCUSSION

Silicon nitrides/ oxynitrides are deposited with CVD method, rather than expensive techniques, such as molecular beam epitaxy. The silicon samples (n-type, 5 Ω-cm, 3 x 1 cm) where cut out of wafers and introduced in the furnace after a rinse with ethanol in an ultrasonic bath. The inside of furnace is cleaned with Ar gas before the experiments. Indeed, we repeated our experiments which Auger electron spectroscopy (AES) technique has been used for getting spectra.

A quartz furnace connected to a gas flow system has been used for the growth of nitride and/or oxynitride layers on Si(100) substrate. The silicon samples are preheated to 1020°C for 10 min in argon gas at a pressure of one atmosphere to remove the native oxide layer. Following this step, dry nitrogen has been allowed into the furnace at one atmosphere pressure. The temperature for nitrogen is 500°C at different nitridation times. Following the nitrogen, argon gas was let into the system at the 500°C and the samples were cooled to ambient temperatures in this gas at one atmosphere pressure. As shown in Figures 1 and 2, there are main peaks at 99, 398 and 510 eV for k_α transition between energy levels of Si, N and O, respectively. The other small peaks around main peaks reveal that other transition between energy levels such as k_β , k_γ , … should also be taken into account. These transitions are demonstrated in sputtering profile (Figure 2) and EDX spectra (Figures 3 and 4). Figure 2 shows that the interfaces between Si/N and Si/O are not sharp, meaning an amorphous structure which is desirable for good gate dielectric (Boucart and Ionescu, 2005; Bahari et al., 2005; Daggubati et al., 2009; Bahari et al., 2006; Zhao et al., 2009; Morgen et al., 2007; Bahari et al., 2008; Hobbs et al., 2002). We have studied EDX spectra with using ZAF method and the results indicate there is not linear background. For this purpose, we have applied X – Powder (Bahari et al., 2009) and ZAF methods. The results which are revealed in Figure 5, give us an accurate thickness of the film. This thickness is less than 10 nm, as estimated from $x = nvt$, where $v = 17$ A°/sec, t is sputtering time between measurements (Figure 2) and n is the number of measurement spectra (Daggubati et al., 2009).

The film thickness in EDX with ZAF method is determined with below relations (Bahari et al., 2006)

$$\frac{I(O_{1s})}{I(Si_{2p})} = \frac{I(O_{1s}\ from\ SiO_2)}{I(Si_{2p}\ from\ Si)} \cdot \frac{1 - \exp\left(-x/2.14\ (nm)\right)}{\exp\left(-x/2.67\ (nm)\right)}$$

$$\frac{I(N_{1s})}{I(Si_{2p})} = \frac{I(N_{1s}\ from\ Si_3N_4)}{I(Si_{2p}\ from\ Si)} \cdot \frac{1 - \exp\left(-x/2.14\ (nm)\right)}{\exp\left(-x/2.67\ (nm)\right)}$$

Where from (Bahari et al., 2006),

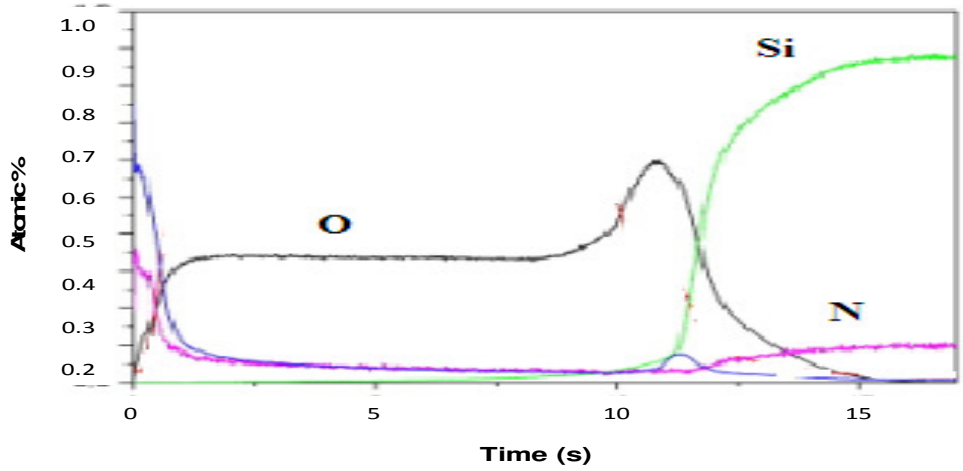

Figure 2. Sputtering profile of silicon oxynitride.

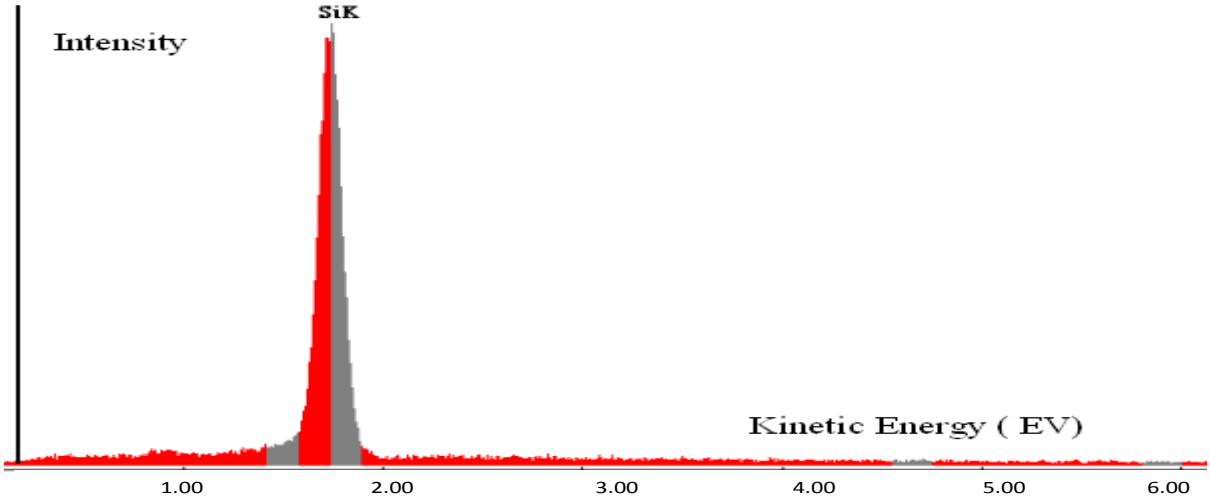

Figure 3. EDX spectrum of the clean silicon substrate.

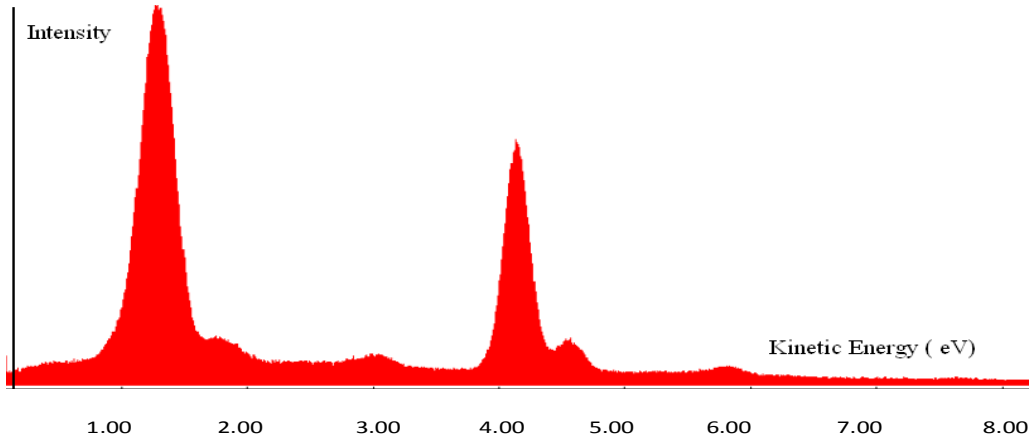

Figure 4. EDX spectrum of the film with using ZAF method.

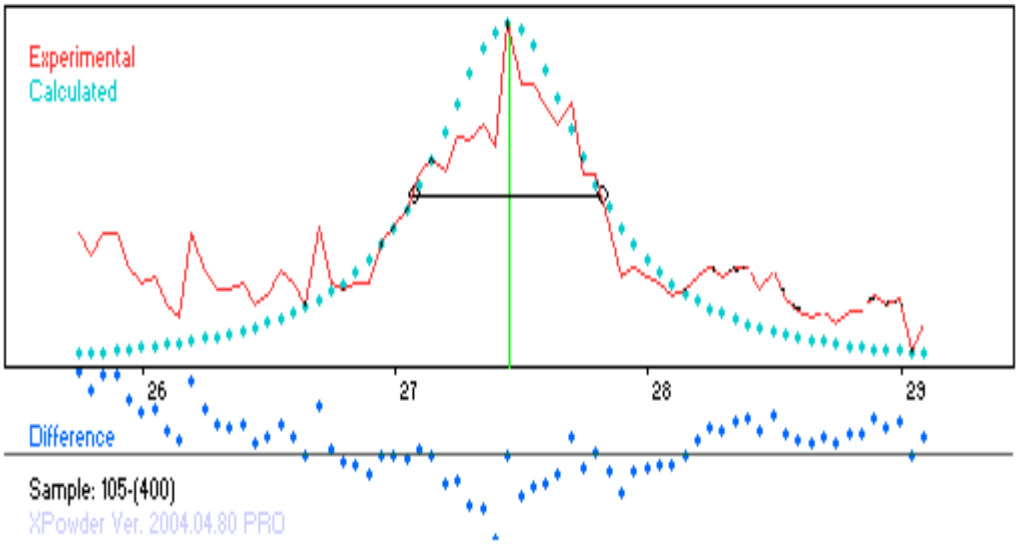

Figure 5. As an example, the correction of determination of a particle size into the film. Dashed line below the background line shows the difference from experimental and calculated data.

$$\frac{I\ (\ O_{1s}\ from\ SiO_2\ )}{I\ (\ Si_{2p}\ \text{from Si}\ )} = 5.1$$

$$\frac{I\ (\ N_{1s}\ from\ Si_3N_4\ )}{I\ (\ Si_{2p}\ \text{from Si}\ )} = 3.1$$

The intensity ratio is found with huge Si, O (and N) intensity in Figures 3 and 4.

As stated previously, we have considered silicon nitride and silicon oxynitride films as DGD and SWCNT as a channel of CNTFET device. We could grow silicon nitride and silicon oxynitride films on the silicon substrate and now we need to study SWCNT as a channel of FET.

Now consider schematic of a CNTFET with source contact passivated by a Si_3N_4 thin film, while the drain is exposed to air. Electrostatic charge balance at non-intimate CNT/electrodes contact can be dominated by adsorbed nitrogen. Due to the surface roughness of the electrodes, a small gap L (about 1 nm) between out could exist, such that a non-intimate Schottky contact is likely to form and the contact Schottky barrier is susceptible to adsorbed nitrogen. In addition to the interface nitrogen layer, we find that dipole polarization along the CNT channel must be considered to establish the electrostatic charge balance of the whole device, from one contact to the CNT, and to the other contact. The main purpose here is study the contact roles in the device (Bahari et al., 2009; Knoch and Appenzeller, 2005). The energy band of the CNT near the contacts must adjust accordingly to restore the charge balance. In the following, a quantitative picture of DGD with four voltage probes is shown (Figure 6) and SWCNT used in this view has a typical diameter of 1.4 nm. Therefore, the CNTs with a Fermi level of 4.7 eV and a band gap E_g of 0.6 eV are considered in this model (Bahari et al., 2009; Knoch and Appenzeller, 2005; Hill et al., 2008; Cale et al., 2008; Wang, 2009). By introducing direct transmission probability of contact p(q) into contact q(p). Therefore, from (Wang, 2009) and the current conservation law, the LB formula, we have:

$$I_p = \frac{2e}{h} \sum_{q \neq p} (T_{q \leftarrow p} \mu_p - T_{p \leftarrow q} \mu_q) \quad (1)$$

In where

$$I_p = \sum_q G_{p \leftarrow q} (V_p - V_q)$$

$$G_{p \leftarrow q} = \frac{2e^2}{h} T_{p \leftarrow q} \quad (2)$$

And

$$V_q = \frac{\mu_q}{e} \quad (3)$$

Where μ and *V* are the chemical potential and the barrier potential at each contact, respectively.

$$\sum_q G_{p \leftarrow q} = \sum_q G_{q \leftarrow p}$$

$$V_p = \frac{\sum_{q \neq p} G_{pq} V_c}{\sum_{q \neq p} G_{pq}}$$

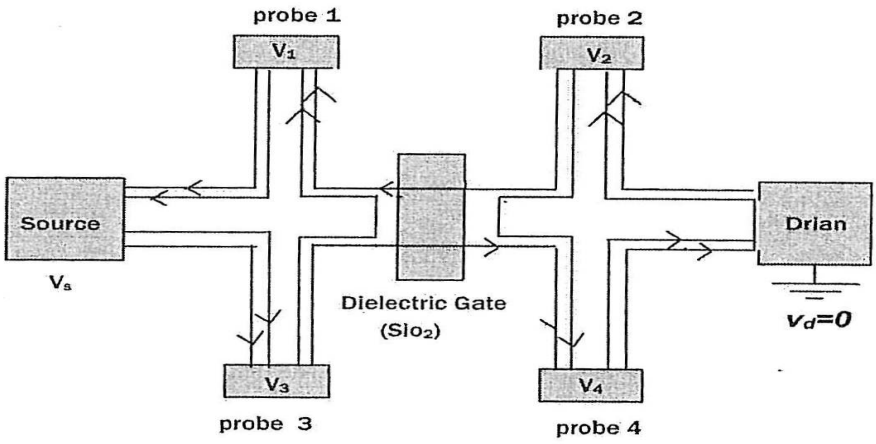

Figure. 6. A quantitative picture of double-gate with four voltage probe (Bahari et al., 2009).

$$G_{pq} \neq G_{qp} \quad (4)$$

On the other hand, for the unpassivated drain contact, positive charges are induced in electrode (σ_e) and CNT (σ_{NT}) to balance the negative nitrogen / oxygen charges (σ_x). The charge neutrality condition can be expressed as follows:

$$\sum_i \sigma_i = 0$$

$$\sigma_e+\sigma_{NT}+\sigma_x = 0 \quad (5)$$

In Equation5, $\sigma_e = \frac{\Delta u\, \varepsilon_g}{ql}$, where q is the unit charge and ε_g is the permittivity of the gap (since the dielectric contact of gases are close to unity, $\varepsilon_g \simeq \varepsilon_o$) and the potential drop across the nano gap, $\Delta u = \phi_s + \phi_o + \xi - \chi_m$ equals to sum of the CNT electron affinity ϕ_o, Fermi level position ξ, the effective work function χ_m and surface band bending ϕ_s.

The work function chosen for the gate contact is assumed to be 4.5 eV corresponding to a metal gate stack (Boucart and Ionescu, 2005). Now, we can get sub threshold swing of a device as the change in gate voltage which should be applied in order to create a, for example, one decade increase in the output current, that is,

$$S = \frac{dV_g}{d(log\, I_d)} \quad (6)$$

The sub threshold swing of a MOSFET is limited by the diffusion current physics of the device in weak inversion, such that the minimum possible swing in an ideal device is

$$S_{MOSFET} = ln(10)\frac{KT}{q} \quad (7)$$

So that, the subthreshold slope for a tunnel FET can be expressed in terms of the gate voltage as

$$S_T = \frac{V_{GS}^2}{5.75(V_{GS}+Constant)} \quad (8)$$

A basic analytical formulation of the tunneling probability T(E), for ultrathin silicon nitride and silicon oxynitride gate dielectrics, has been delivered in the study in (Wang, 2009) and shows that:

$$T(E) \propto \exp\left(-\frac{4\sqrt{2m^*}\, E_g^{\frac{3}{2}}}{3\theta\hbar(E_g+\Delta\phi)}\sqrt{\frac{\varepsilon_N}{\varepsilon_{Si}}}\, t_N t_{Si}\right)\Delta\phi \quad (9)$$

Where m^* is the effective carrier mass, E_g is the band gap, $\Delta\phi$ is the energy range over which tunneling can take place, and t_N (t_{ON}), t_{Si}, ε_N (ε_{ON}) and ε_{Si} are the nitride (oxynitride) and silicon film thickness and dielectric constants, respectively. It is clear from Equation 9, that in contrast with a MOSFET, a material with higher band gap, dense, high-k dielectric such as Si_3N_4 and/or SiO_xN_y can be suggested for the future of FET transistor devices.

CONCLUSION

The obtained results show that the DG leakage current in silicon nitride and/or oxynitride is significantly lower than that in silicon dioxide of the same equivalent oxide thickness. It means that silicon nitride films can exhibit very strong resistance to boron penetration. We suggest these gate dielectrics to complement or replace MOSFET technology.

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