International Journal of the Physical Sciences Vol. 6(30), pp. 6946 - 6957, 23 November, 2011
Available online at http://www.academicjournals.org/IJPS
DOI: 10.5897/IJPS10.665
ISSN 1992 - 1950 ©2011 Academic Journals

Full Length Research Paper

Simulation analysis of 2.4 GHz MEMS/NEMS voltage controlled oscillator

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Accepted 13 June, 2011

This paper presents the design and analysis of a novel 2.4 GHz Voltage Controlled Oscillator (VCO), with amplitude control and Q enhancement circuit, for wireless communication applications. The variable capacitors and the inductors were designed using ANSYS and imported through DAC components in ADS (Advanced Design software). Accurate simulation of the VCO was performed in the software environments and the results are provided. To enhance the quality factor and to control the oscillation amplitude, additional CMOS circuits have been implemented. This VCO operates at 2.4 GHz, achieves a phase noise of -119dBc/Hz, 3 MHz far from the carrier frequency. The VCO produces frequency tuning from 1.82 to 2.60 GHz (32.5%) with an ultra low power consumption of 73 µW. The output power level of the VCO is -9 dBm, with an improved predicted quality factor of 77.

Key words: Variable capacitor, nano inductor, voltage controlled oscillator, phase noise, Q enhancement.

INTRODUCTION

Low power, low voltage integrated circuits have received stringent requirements in the area of modern communication circuits such as wireless transceivers, filters, low noise amplifiers and high frequency oscillators. With the demand of wide band width and high speed communication channels, wireless transceivers, especially those working in GHz frequencies, call for voltage controlled oscillator (VCOs) with outstanding performance (Jan and Michiel, 1997; Gu, 2005). The performance properties of the VCOs are phase noise, frequency tuning range, power consumption, tuning sensitivity, spectral purity, load pulling, supply pulling, output power, harmonic suppression, output oscillation amplitude, and chip size. With the advancements in micromachining techniques the chip size can be reduced to several micro meters (Wang et al., 2005).The tuning range of the VCO depends on the frequency (capacitive and inductive) tuning elements like capacitors and inductors. By integrating these elements on single chip together with CMOS components, the tuning range may be improved (Ryckaert et al., 2005; Li et al., 2005; Tseng et al., 2007). The performance measure of an oscillator is its quality factor, that is, the ratio of the resonant frequency peak to its spectral bandwidth.This performance indicator can be improved by decreasing the phase noise, since quality factor and the phase noise are inversely proportional to each other. Several works had been demonstrated to improve the major performance factors such as power consumption (Wang and Luong, 2008; Hsieh and Lu, 2007) and phase noise (Jeong and Yoo, 2006; Lee et al., 2007). The objective of this paper is to develop a VCO which operates with considerable improvement in all these factors.Parallel-plate MEMS variable capacitors along with a discrete commercially available 8.2 nH inductor and a separately-fabricated CMOS circuit were attached to a test board surface and wire-bonded to form the VCO (Young and Boser, 1997). This prototype oscillated at a center frequency of 714 MHz and could be tuned from 707 to 721 MHz over a DC voltage of 5.5 V. The phase noise was -107 dBc/Hz at an offset frequency of 100 kHz. Another VCO prototype with the same MEMS variable capacitors and a 5 mm-long bond wire 6 nH inductor were tested. It achieved -105 dBc/Hz phase noise at 100 kHz offset frequency from a

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Abbreviations: MWCNT, Multi walled carbon nano tube; **VCO,** voltage controlled oscillator; **ADS,** advanced design software.

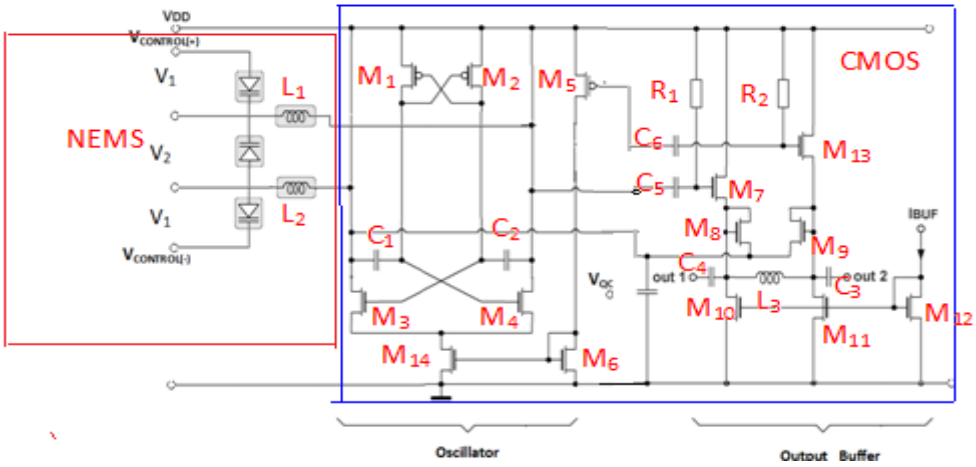


Figure 1. Proposed differential VCO topology with the MEMS and CMOS components.

1.028-GHz carrier. The oscillator could be tuned over 20 MHz with 3 V and consumed 3.8 mA from a 3.3 V supply (Young et al., 1999). A 1.9-GHz CMOS VCO prototype, where the resonant circuit consisted of micromachined electromechanically tunable capacitors and a 3.5 nH bond wire was imple-mented in a MUMPs polysilicon surface micromachining process. The active circuits were fabricated using a 0.5 µm CMOS process. The VCO was assembled in a ceramic package where the MUMPs and CMOS chips were connected using wire bonds. The experimental VCO achieved a phase noise of -98 and -126 dBc/Hz at 100 and 600 kHz offsets from the carrier, respectively. The tuning range of the VCO was 9%. The VCO circuit and the output buffer consumed 15 and 30 mW from a 2.7-V power supply, respectively (Young et al., 2001; Dec and Suyama, 2000a, b).

Table 1. Design parameters used for the simulation.

Parameter		Design values used for the simulation
MOS Transistors (W/L) ratio	M_3	12.5 µm/ 0.9 µm N=50
	M_4	12.5 µm/ 0.9 µm N=50
	M_1	6 µm/ 0.6 µm N=30
	M_2	6 µm/ 0.6 µm N=30
L_P (Inductance)		0.61 nH
Micro Scale varactor		9.5 pF
C_1 (Capacitance)		10 µF
I_{bias} (Bias Current)		2.8 mA
R_P (Parallel resistance)		150 Ω
g_m		≥ 6.67 mS + (safety factor 1.5)

MATERIALS AND METHODS

Circuit design

The LC VCO was designed to oscillate at 2.4 GHz, and to determine the impact on the performance parameters. The cross coupled differential topology is utilized for the design to achieve large output voltage swing. From the well known theory of oscillators, the positive feedback transistors M_3 and M_4 are used to achieve negative input resistance, with which positive resistance of LC resonant circuit might be eliminated bringing on zero-dampen oscillating property. MOS transistors M_6 and M_{14} provide DC offset to the differential pairs. The output of the VCO is passed through a band pass filter to reduce the out-of-band noise level of the output signal. A resonant circuit with high quality factor, Q, is necessary to obtain low phase noise and is realized using Micro/Nano Electro Mechanical elements. The MOS transistors (M_1-M_{13}), the fixed capacitors (C_1-C_6), the inductor (L_3), and the resistors (R_1, R2) are realized using CMOS technology. An output buffer circuit, I_{BUF}, is designed to deliver maximum power to 50 ohms load. Figure 1 shows the schematic of the proposed VCO. The MEMS and CMOS components are differentiated in Figure 1.

The design of the oscillator is based on the principle of negative transconductance ($-g_m$) oscillator theory. A cross-coupled CMOS differential topology was chosen as the preferred topology because of its low phase noise performance. VCOs are generally designed for minimum phase noise under the constraints of dc power dissipation, tuning range, output voltage swing and die area. The dc power dissipation is given by $V_{supply} I_{bias} \leq P_{dissipationmax}$. The magnitude of the output voltage at the drains of the NMOS transistors is governed, to first order, by the ac impedance of the lossy tank: $V_{tank} \approx I_{bias} R_p$ where $R_p = Q_L \omega_o L$ and V_{tank} is the single-ended peak-to-peak voltage swing at either the + or - output node of the VCO before any output buffering. To increase the voltage swing V_{tank}, the bias current I_{bias} is set to an appropriate value, which is found to be 2.8 mA after several iterations. The NMOS transistors are biased and laid out such that the required g_m is obtained to overcome all losses, including those of the tank and the transistors. The primary goal in the design of the oscillator is to size (design) the active devices to overcome the losses associated with the tank parallel resistance, Rp. The losses associated with the tank inductance (L = 0.61 nH) and capacitance (C = 9 pF) can be represented by the parallel resistance, Rp = 150 Ω (obtained from inductor and varactor design simulations). Furthermore, the following parameters are used in the simulation to achieve better performance (Table 1).

Figure 2 illustrates the complete circuit of the designed VCO including the amplitude control, Q enhancement and out buffer circuits. The Quality factor of the oscillator performance is deter-mined by the quality factor of the resonant circuit. The resonant

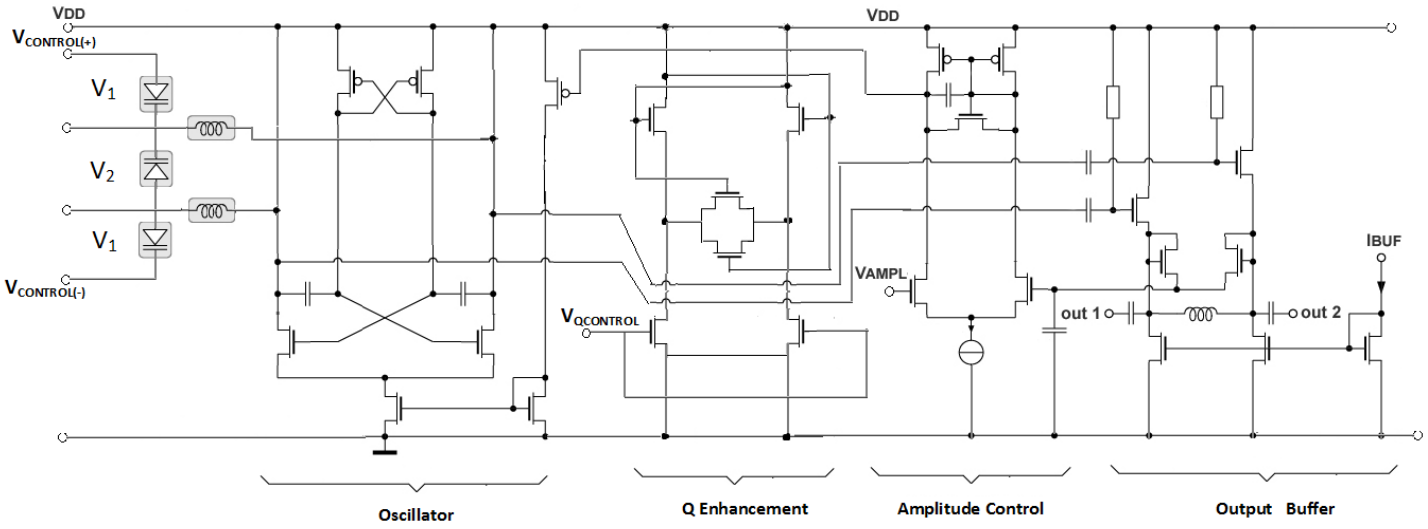


Figure 2. Schematic of the differential VCO topology with Q enhancement and amplitude control.

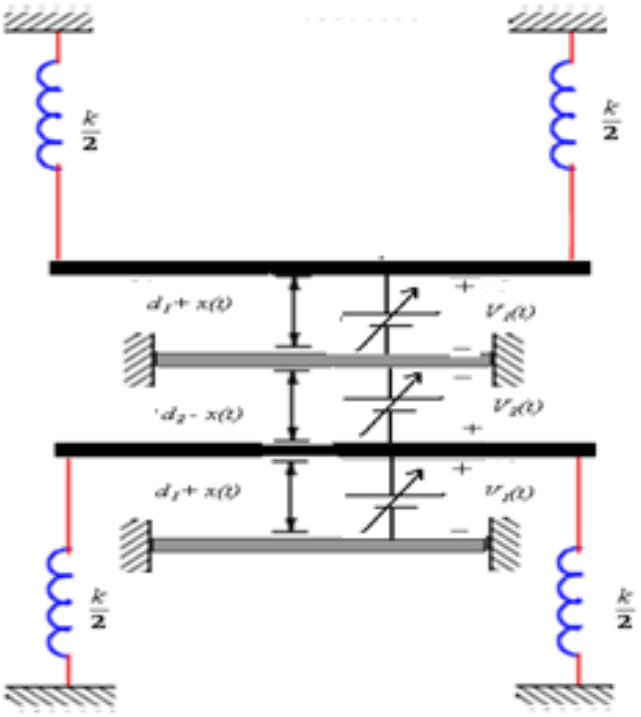


Figure 3. Microscale capacitor structure.

circuit implemented in this circuit is imported from ANSYS to ADS through its DAC import feature. For the simulation, CMOS and the other discrete component models utilized the ADS component library. Figure 3 illustrates the design of the capacitor model. The proposed structure has two movable plates and two fixed plates. The four plate structure is actuated with two supply voltages, v_1 and v_2. The two shorter plates, shown in grey, are fixed. The two longer plates, shown in black, are suspended using springs. Each suspended plate uses two springs with spring constant k/2 each. When bias voltages are applied to the plates, the suspended plates are attracted to the opposite polarities. When a dc voltage, v_1, is singularly applied to the plates, the top and bottom suspended plates move in a manner relative to the fixed plates and produce the desired increase or decrease in capacitance. When a dc voltage, v_2, is singularly applied to the bottom suspended plate, it moves upwards to the fixed plates. The movement of the plates is due to the electrostatic force produced by the bias voltage. The force due to the spring under equilibrium condition can be written as:

$$2kx = \frac{dC_d}{dx} v_1^{\,2} + \frac{1}{2}\frac{dC_p}{dx} v_2^{\,2}$$

$$= -\frac{\varepsilon_d A v_1^2}{(d_1 + x_{V1})} + \frac{1}{2}\frac{\varepsilon_d A v_2^2}{(d_1 - x_{V2})} \quad (1)$$

Where C_d is the desired capacitance, x is the displacement due to the applied voltage, A is the area of the capacitor plates, d_1 ,d_2 are the distance between the capacitor plates when the applied voltages are zero, and ε_d (= $\varepsilon_a \varepsilon_0$) is the dielectric constant of air. The maximum tuning value of the capacitor is 3 $C_{d,}$ and the minimum tuning value of the capacitor is 3 C_d /2. The desired capacitance when both the supply voltages are zero is 8 pF and d_1 and d_2 are equal. The performance of the four layer microscale variable capacitor are further documented (Sreeja and Radha, 2010a, b).

Figure 4 shows the structure of Multi Walled Carbon Nano Tube (MWCNT) based pulse inductor (Sreeja and Radha, 2011). The proposed structure is in the form of pulse. Since MWCNTs have many shells in parallel, the effective resistance and kinetic inductance can be given as:

$$R_{MWCNT} = \frac{1}{\sum_{i^{th}shell} \frac{1}{R_{CNT}^i}}$$

$$L_{kCNT} = \frac{L_k}{\sum_{i^{th}shell} \frac{1}{R_{CNT}^i}} \quad (2)$$

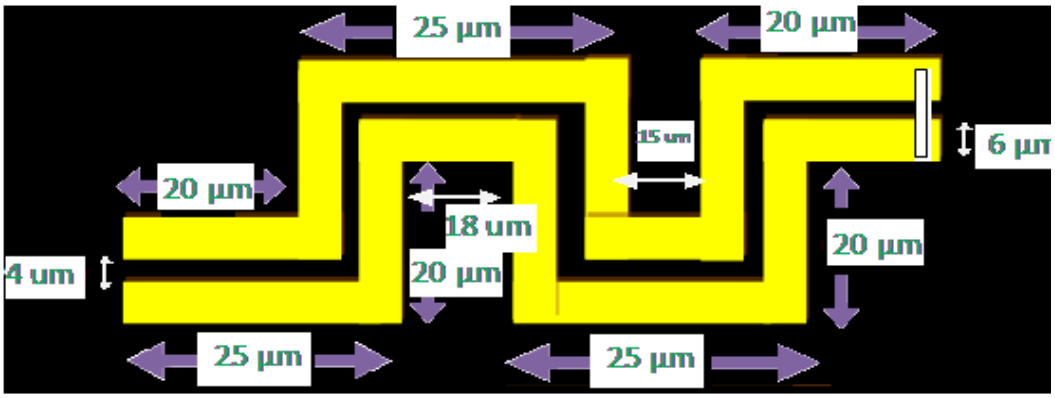


Figure 4. Nanoscale inductor structure.

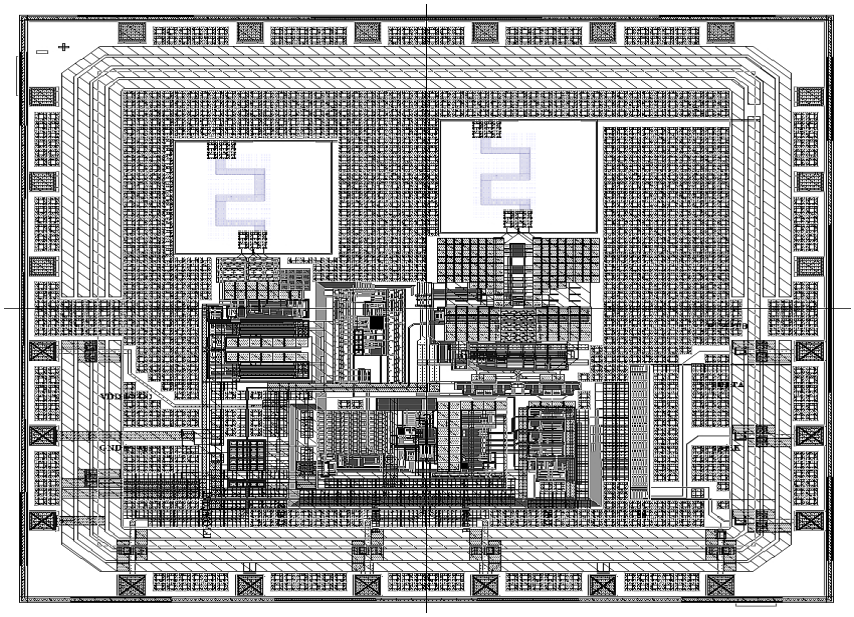


Figure 5. Layout of the VCO.

Where R_{CNT}^{i} is the effective resistance of i[th] shell, and L_k is the kinetic inductance. The magnetic inductance and the electrostatic capacitance of each segment of the conductor can be calculated from the relations:

$$L_m = \frac{\mu_0 l}{2\pi}\ln(\frac{D}{d})$$

$$C_e = \frac{2\pi\varepsilon}{\ln(\frac{D}{d})} \quad (3)$$

Where *l* is the length of the segment, *d* is the distance between the conductor segments, ε is the dielectric constant of the conductor material, and μ_0 *is* the permeability of the conductor material.The Q factors of the simulated inductor and capacitor at 2.40 GHz are 186 and 75, respectively. In addition to this a Q enhancement circuit is designed to improve the quality factor of the VCO. Improvement in Q is achieved by increasing the bandwidth of the oscillation. The enhancement circuit increases the band width with respect to the applied dc voltage $V_{QCONTROL}$. The range of this voltage must be less than the supply voltage V_{DD}. The simulation analysis software ADS is used to investigate the parameters of the designed circuit. The performance parameters are extracted using Harmonic Balance (HB) method (Brambilla et al., 2009) in order to analyze the periodic stability of the oscillator accurately. The amplitude control circuit maintains the maximum output versus amplitude supply voltage V_{DD}.

LAYOUT DESIGN

Layout of the proposed VCO is designed using a 90 nm CMOS process in Microwind environment**.** The chip layout is illustrated in Figure 5. The CMOS section of the VCO structure is symmetrical. The layout area of the VCO is 350 x 380 µm**,** including the bonding pads. The distance between the components is minimized in order

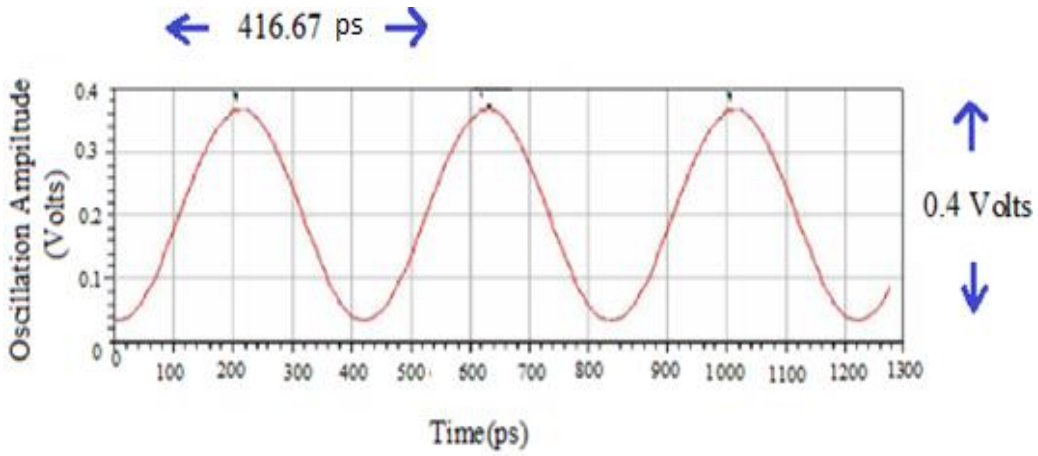


Figure 6. Output oscillations of VCO circuit simulated using ADS.

to reduce the phase noise, and the layout is made as symmetrical and compact as possible to ensure differential operation and reduce parasitic inductance or capacitance.

RESULTS

Performance analysis

The time referenced oscillation shown in Figure 6 is generated in ADS environment using the cross coupled VCO topology. The oscillation frequency is measured as 2.40 GHz, with the variable capacitor tuning voltage v_1 at 0.072 volts, and v_2 at 0.9 volts. All simulations are performed with 0.6 volts power supply voltage and a current consumption of 3.2 mA in the core circuit. The simulation results of phase noise using HB method with ADS is shown in Figure 7. Since the proposed VCO is operated under ultra low dc voltage, the cross coupled transistors are potentially biased in the weak inversion region. Therefore the electrical noise is the main source of the VCO noise, rather than thermal noise. The phase noise is simulated as -119 dBc/Hz at an offset frequency of 3 MHz far from the carrier frequency. It is noted that for low power operations, the cross coupled transistors may contribute more noise to the LC tank as the supply voltage decreases. Hence, it imposes a fundamental limitation on the phase noise of the VCO for ultra low power and low voltage application.

The tested circuit is tranferred to the layout for further simulation. Layout shown in Figure 5 is simulated, and the simulation results are shown from Figures 8 to 12. Figure 8 shows the simulation results when v_1 is varied from 0-0.3 volts and v_2 is kept at 0.9 volts. When the control voltage is increased above $V_{dd}/2$ (0.3 volts), the device stops oscillating, and a dc voltage of 0.6 volts is produced as output voltage. Thus, the maximum level of the control voltage is $V_{dd}/2$. Figure 9 shows the Output oscillations of VCO layout simulated when the control voltage is 0.072 volts. Figures 10 and 11 shows the current waveforms of PMOS and NMOS transistors, respectively. The transistors are sized to achieve the design specifications. The power consumption of the device with a supply voltage of 0.6 volts is approximately 73 µW. The device is simulated with a power supply voltage of 1.2 volts and the current consumption is found to be 0.369 mA. Also, during the simulations, it is noted that the phase noise has an inverse relation with the supply voltage. The phase noise may be improved at higher supply voltages. Figure 12 shows the spectrum of VCO with a center frequency of 2.4 GHz. Table 2 shows the comparison of the simulated results with the previously published measurement resuts. As in the table table, the designed VCO exibits a tuning frequency range of 780 MHz, with 2.4 GHz as center frequency which leads to a tuning percentage of 32.5. The tuning range is even greater, since the micro scaled varacters have wide tuning range. Because of the trade off between the phase noise and the tuning frequency range, that is, the phase noise of the oscillator is inversly propotional to the tuning frequency range, the tuning frequency range is limited. The tank circuit impedance exibits an inversely proportional relationship with the oscillation frequency, when the tank circuit impedance is lowered, the start up gain is reduced as well as output voltage swing. Hence, the value of the tank circuit impedance is carefully chosen to avoid these issues. The quality factor of the resonant circuit at 2.4 GHz is calculated as 69, which provides a quality factor of 63 for the VCO at the same frequency. With the additional circuitry included, the quality factor of the VCO has been improved to 77 at 2.4 GHz. The gate-source and the drain source capacitance of the PMOS and NMOS transistors are measured between 0 to 3.5 fF. Figure 13 shows the VI characteristics of the MOS trasistors.

Conclusion

A 2.4 GHz VCO is simulated and the results of the

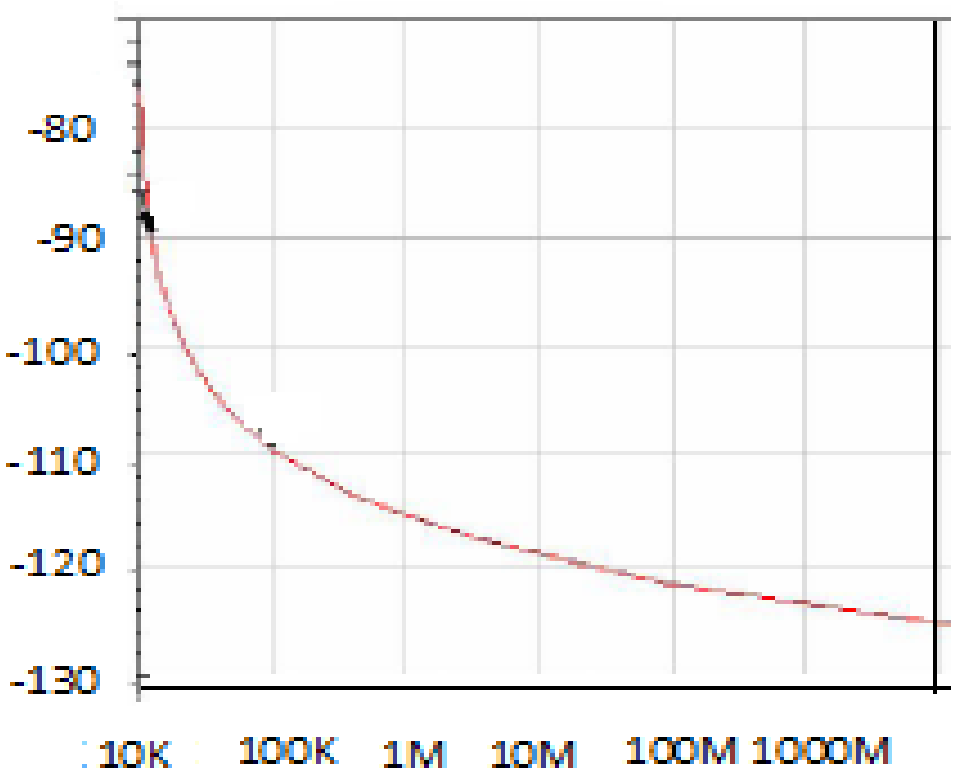


Figure 7. Simulated phase noise as a function of frequency.

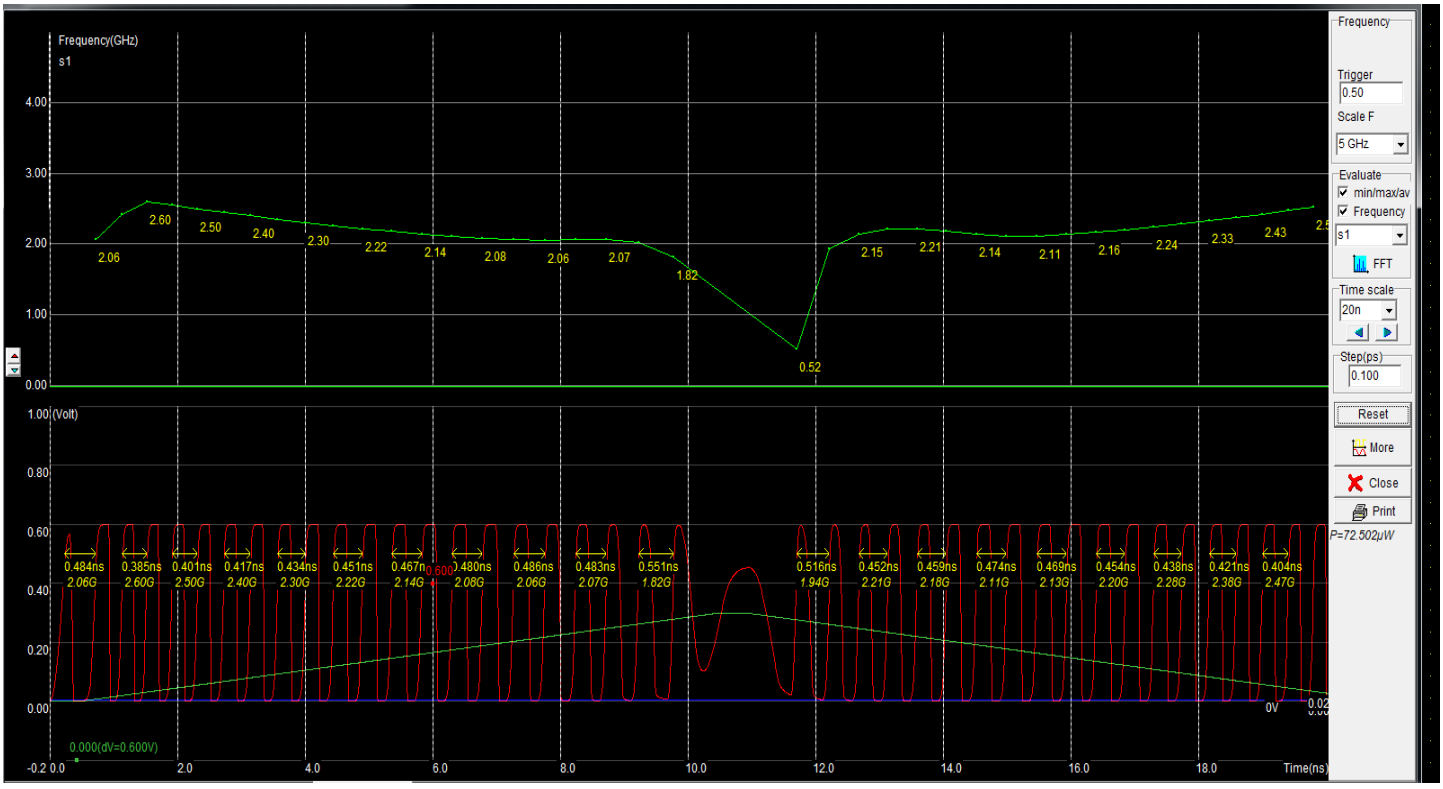


Figure 8. Output oscillations of VCO layout simulated using Microwind- Control voltage v_1 varies from 0 volts to 0.29 volts and v_2 is kept at 0.9 volts.

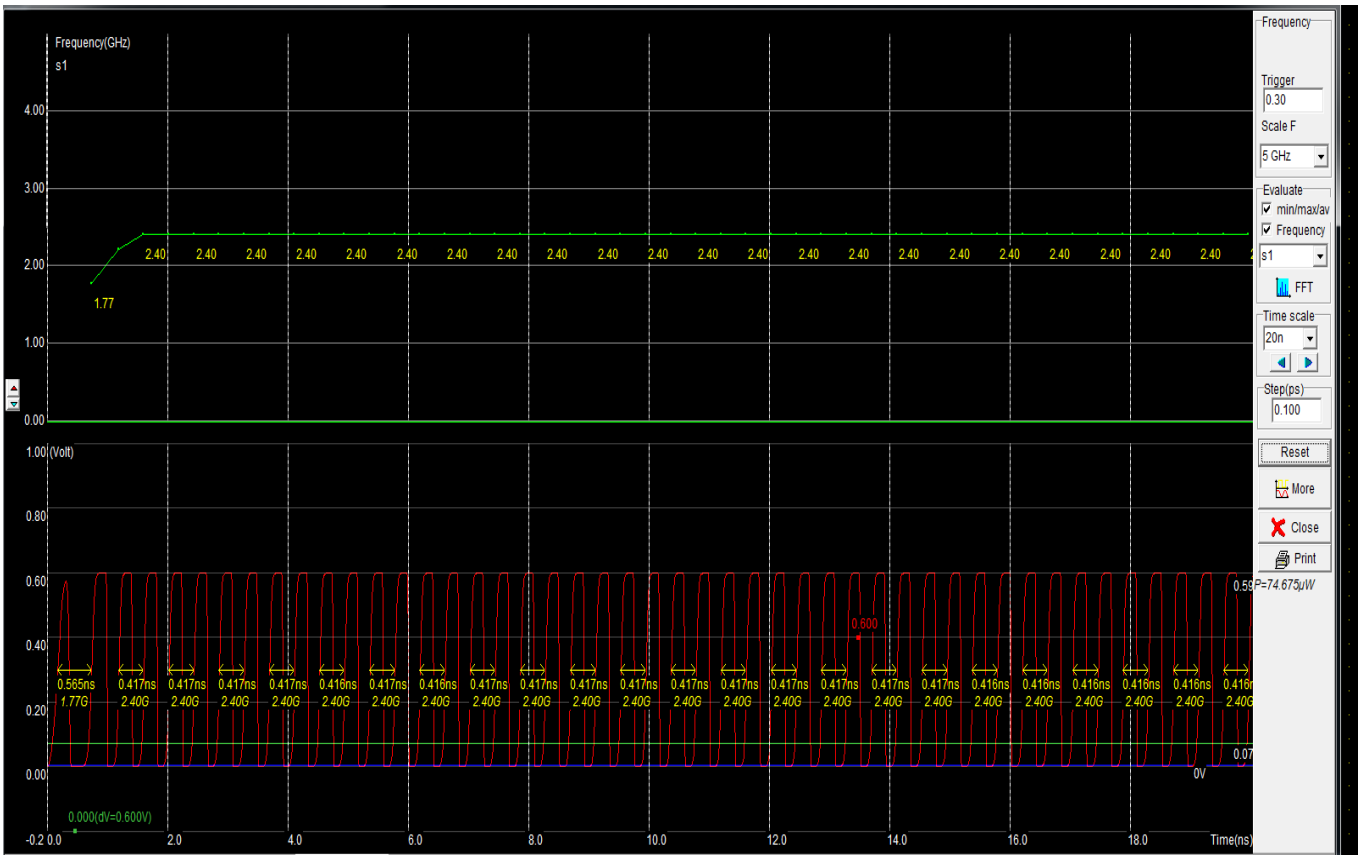


Figure 9. Output oscillations of VCO layout simulated using Microwind-Control voltage is 0.072 volts.

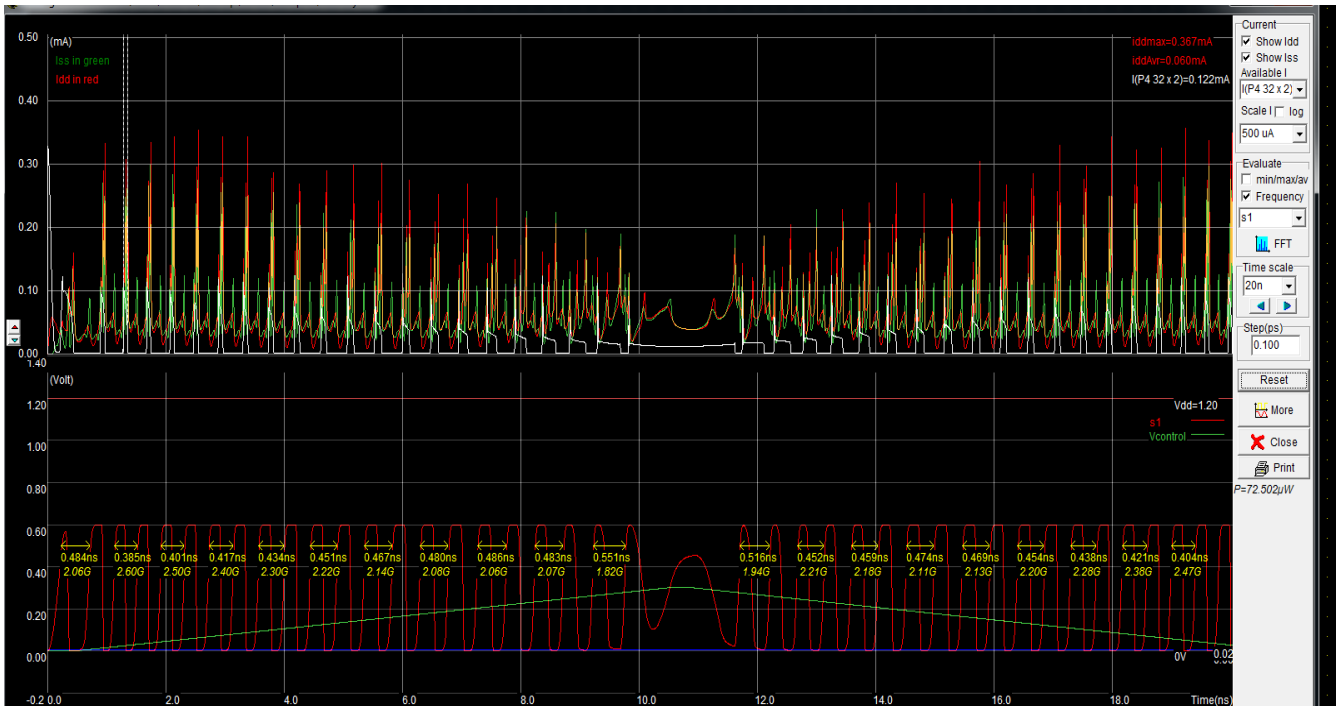


Figure 10. Output voltage and current waveforms(PMOS) of VCO layout simulated using Microwind-Control voltage varies from 0 volts to 0.3 volts.

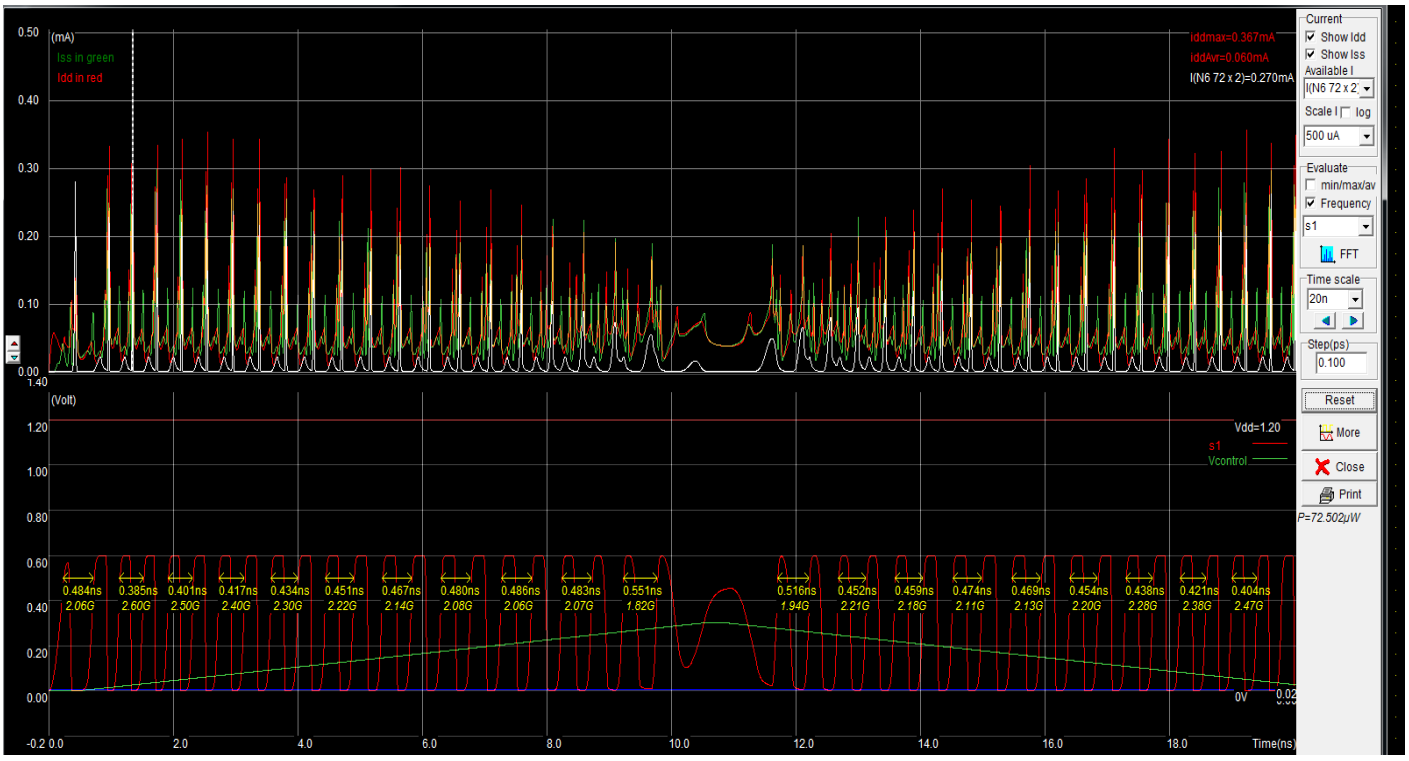


Figure 11. Output voltage and current waveforms(NMOS) of VCO layout simulated using Microwind-Control voltage varies from 0 volts to 0.29 volts.

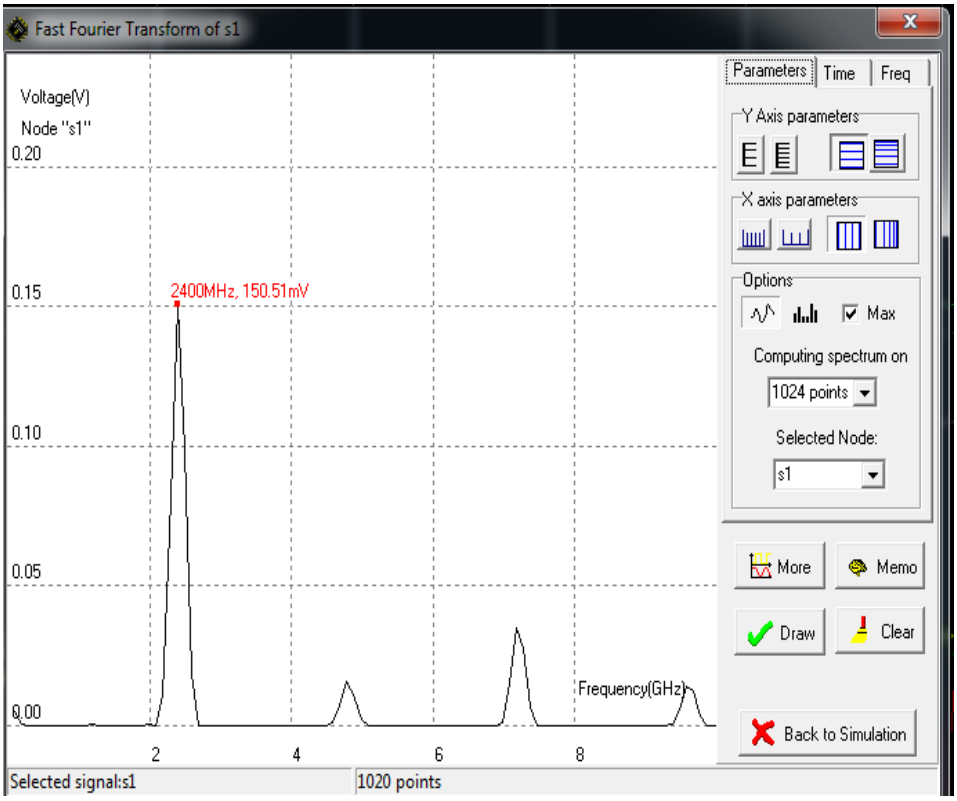
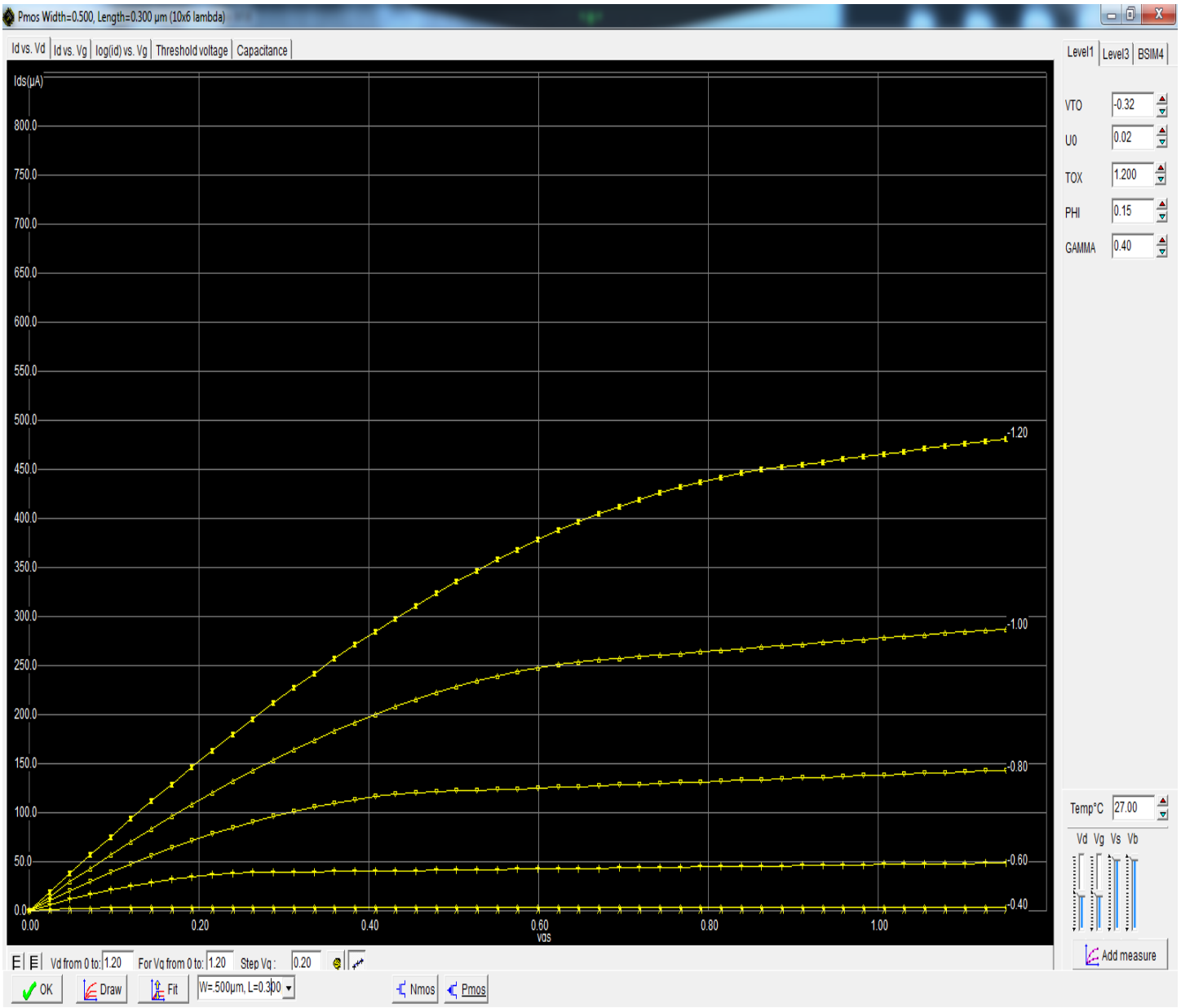


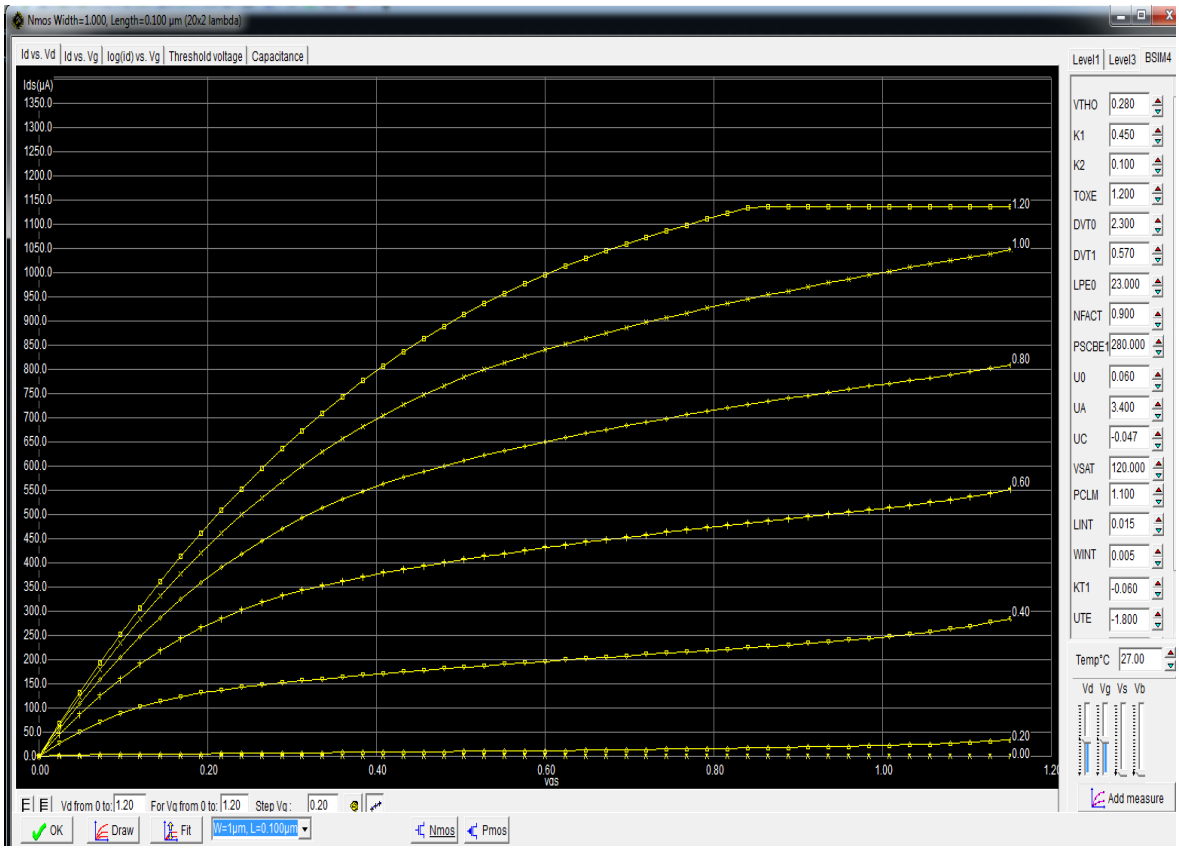
Figure 12. Frequency spectrum of VCO when control voltage v_1 is equal to 0.072 volts.

Table 2. Simulated Results of VCO.

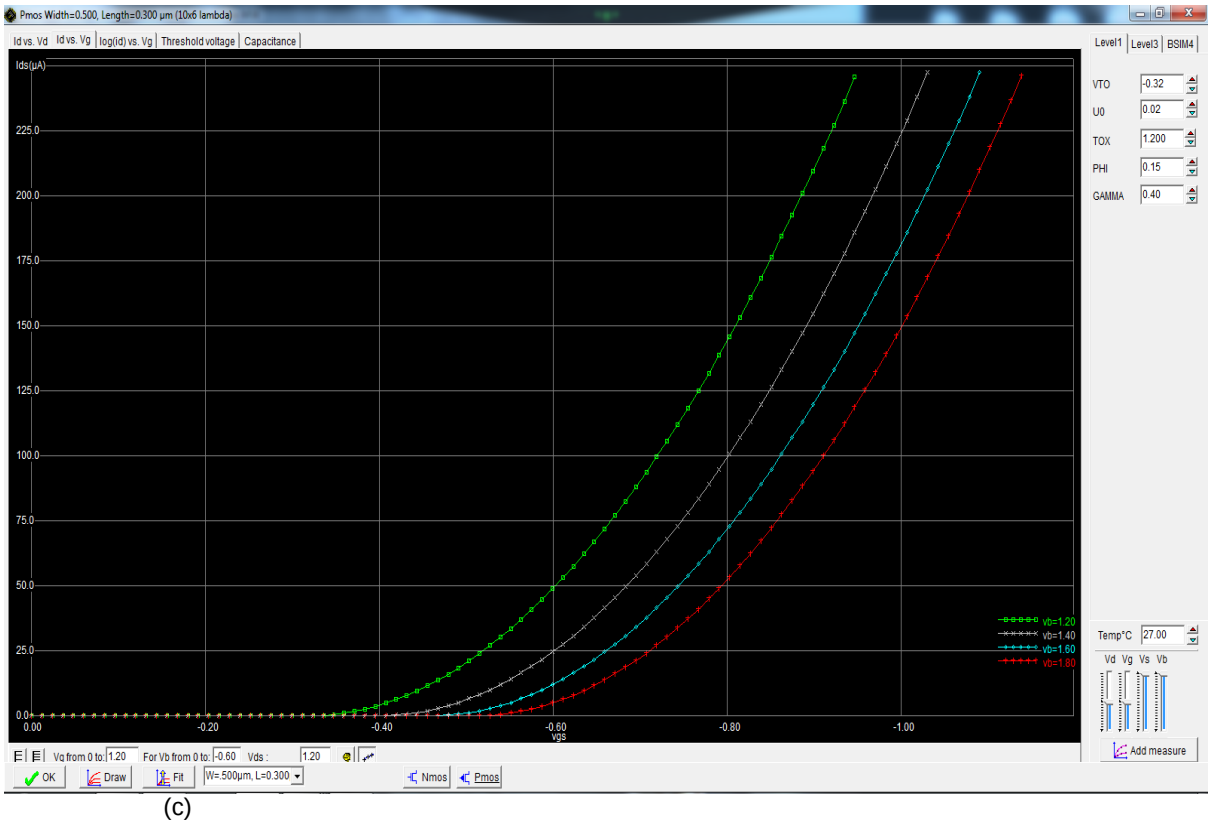
Parameter	This work	Dec and Suyama (2000a, b)	Ramachandran et al. (2004)	Park et al. (2003)	Chen et al. (2005)
Tuning range (%)	32.5	3.4	30	70	15.6
Center frequency (GHz)	**2.40**	**2.4**	**2.45**	**2.6**	**2.78**
Phase noise (dBc/Hz @ 600 kHz)	-109	-120	-118	-124	-121
Power consumption	73 µW	-	3.5-5 mW	-	-
Output power (at 50 Ω load) dBm	-9	-14	-4	-	-14.4
Supply voltage (volts)	0.6	2.7	3.3	3	
Tuning voltage range (volts)	0-0.3	2.7-8.7	5.5	4.5	0-3
Quality factor (VCO) (@ 2.4 GHz)	77	-	-	-	-



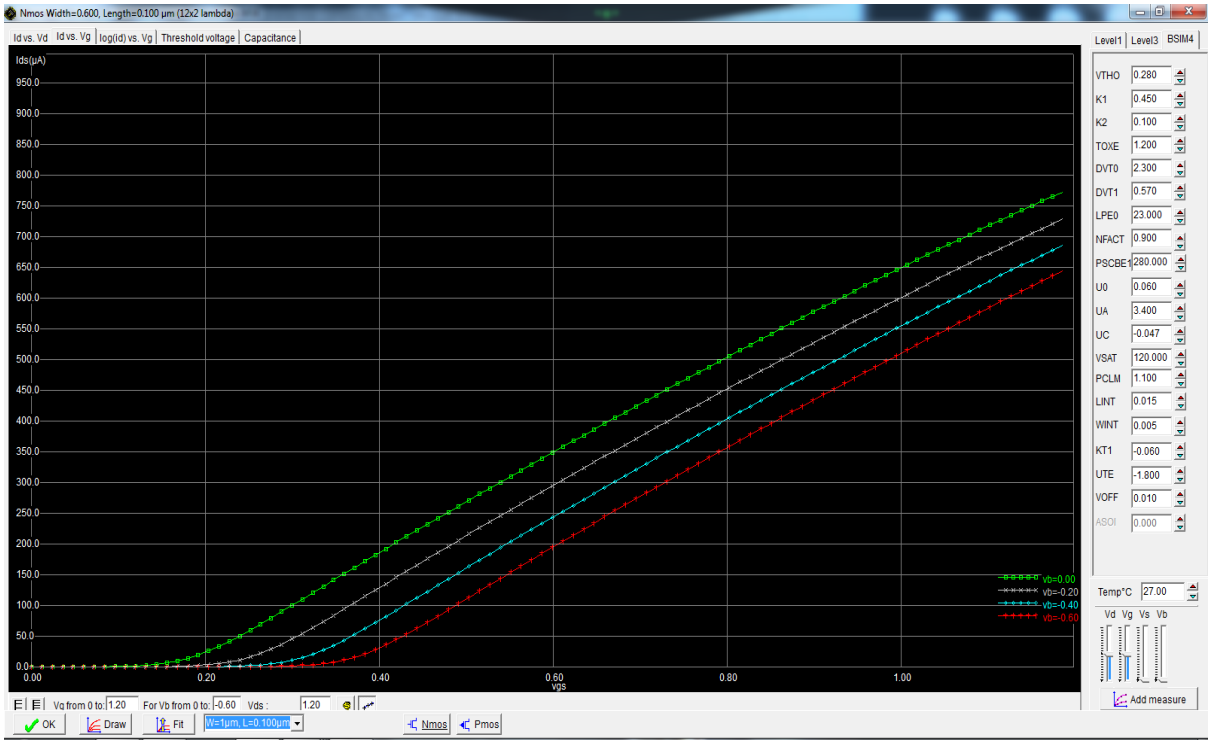
(a)


Nmos Width=1.000, Length=0.100 µm (20x2 lambda)
Id vs. Vd
Id vs. Vg
log(id) vs. Vg
Threshold voltage
Capacitance
Ids(µA)
vgs
1.20
1.00
0.80
0.60
0.40
0.20
0.00
Level1
Level3
BSIM4
VTHO 0.280
K1 0.450
K2 0.100
TOXE 1.200
DVT0 2.300
DVT1 0.570
LPE0 23.000
NFACT 0.900
PSCBE1 280.000
U0 0.060
UA 3.400
UC -0.047
VSAT 120.000
PCLM 1.100
LINT 0.015
WINT 0.005
KT1 -0.060
UTE -1.800
Temp°C 27.00
Vd Vg Vs Vb
Add measure
Vd from 0 to: 1.20
For Vg from 0 to: 1.20
Step Vg: 0.20
OK
Draw
Fit
W=1µm, L=0.100µm
Nmos
Pmos

(b)


Pmos Width=0.500, Length=0.300 µm (10x6 lambda)
Id vs. Vd
Id vs. Vg
log(id) vs. Vg
Threshold voltage
Capacitance
Ids(µA)
vgs
vb=1.20
vb=1.40
vb=1.60
vb=1.80
Level1
Level3
BSIM4
VTO -0.32
U0 0.02
TOX 1.200
PHI 0.15
GAMMA 0.40
Temp°C 27.00
Vd Vg Vs Vb
Add measure
Vg from 0 to: 1.20
For Vb from 0 to: -0.60
Vds: 1.20
OK
Draw
Fit
W=.500µm, L=0.300
Nmos
Pmos

(c)



(d)

Figure 13. VI characteristics of MOS transistors simulated on the layout (a) Output characteristics (drain) of PMOS (b) Output characteristics (drain) of NMOS (c) Input characteristics (source) of PMOS (d) Input characteristics (source) of NMOS.

simulation are analysed. The results indicated VCO operation at a centre frequency of 2.4 GHz with a quality factor of 77. The chip size is 350 x 380 µm. The simulation predicts phase noise of -119 dBc/Hz at a power supply voltage of 0.6 volts. The simulated oscillation amplitude is maintained at V_{dd} using the amplitude control circuit. The simulation operational conditions indicate that the device consumes ultra low power at 73 µW, including the buffer, amplitude control and Q enhancement circuit. Further, the fabrication of the VCO is expected.

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