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Full Length Research Paper

Frequency synthesis techniques for high speed communication system

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The phase locked loop (PLL) has been widely used in wireless communication systems due to the high frequency resolution and the short locking time. In particular, it is possible to achieve a very high-frequency resolution together with fast settling and spectral purity. We used DDS and two types of PLLs analog as well as digital in our work. Though we gave a comparative results of PLLs used in our simulation based on their settling time. Second frequency technique, the Direct Digital Frequency Synthesis (DDFS) is a kind of frequency synthesizer that uses electronic methods for digitally creating arbitrary waveforms and frequencies from a single, fixed source frequency. DDFS is a mixed signal part. DDFS's digital part is also known as Numerically Controlled Oscillator, which consists of a Phase Register, a Phase Accumulator and a ROM. The analog part has Digital-to-Analog Converter and a filter. NCO is a digital computing block which renders digital word sequences in time at a given reference clock frequency fclk, which thereafter are converted into analog signals to serve as a synthesizer. In this work we analyzed the simulated results of DDS and the different PLLs used for frequency synthesis using tools Xilinx and Matlab.

Key words: Phase locked loop (PLL), Direct Digital Synthesis (DDS), communication system, frequency synthesis.

INTRODUCTION

The phase locked loop (PLL) is a fundamental part of radio, wireless and telecommunication technology. PLL is a simple feedback architecture that allows economic multiplication of crystal frequencies by large variable numbers. By studying the loop components and their reaction to various noise sources, we will show that PLL is uniquely suited for generation of stable, low noise tunable RF signals for radio, timing and wireless applications. Some of the main challenges fulfilled by PLL technology are economy in size, power and cost while maintaining good spectral purity (Bar-Giora, 1999).

In all PLL applications, the phase-locked condition must be achieved and maintained. In order to avoid distortion, many applications require operation in the linear region, that is, the total variance of the phase error process resulting from noise and modulation must be kept small enough. If the PLL operates in the linear region then the linearized base band model may be used in circuit design and development. Recall that only the PD output, VCO control voltage, input phase and output phase appear in the PLL based and model. All these signals are low-frequency signals (Telba et al., 2004).

In this work, the phase-locked loop and its block design are demonstrated. A PLL block is the core of our frequency synthesizer design and because it is a system containing many analog sub-circuits, it can be used to test the designer's analog expertise. Also, since it has many design constrains that will be shown in the following as follows; a full-custom design flow for the PLL block layout is used. The basic concepts of PLLs with simple block diagrams and equations are introduced. We also discuss the various PLL parameters (Frequency range or tuning bandwidth, step size or frequency resolution, phase noise, spurious signal level, loop bandwidth, switching speed, size, power, supply voltage, interface protocol, temperature range and reliability) and PLL components (VCO, crystal oscillators, dividers and phase detectors). The PLL is a very interesting and useful building block available as single integrated circuits from

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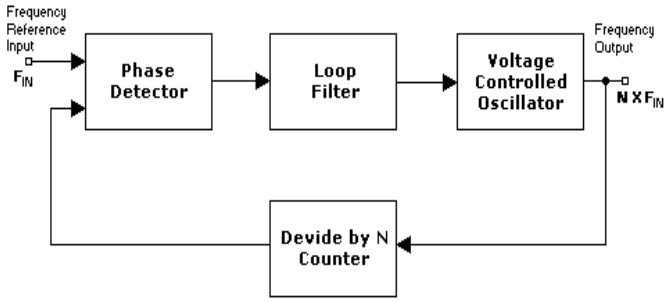


Figure 1. PLL block diagram.

several well known manufacturers. It contains a phase detector, amplifier, and VCO, as represents a blend of digital and analog techniques all in one package (Milan, 2003). One of its many applications and features is tone-decoding.

Also, in this work, the digital frequency synthesis approach employs a stable source frequency that is reference clock to define times at which digital sinusoidal sample values are produced. These samples are converted from digital to analog format and smoothed by reconstruction filter to produce analog frequency signals. A DDFS typically consists of a phase accumulator (PA) and a sine lookup table (LUT). The input to the phase accumulator is a frequency control word, which determines the periodicity of the phase accumulator. The PA is updated to the frequency control word or tuning word, at each clock, the output of the PA is fed to the LUT. The output of the LUT is then converted to an analog signal using a digital to analog converter. The size of the LUT depends on the length of the n-bit PA. If n is large then the LUT becomes too large, which is not desirable. This slows down the speed of the DDS and results in higher power consumption. To reduce the size of the LUT, a technique of phase truncation (PT) is employed. Since in this technique part of the phase generated by the PA is truncated that gives rise to spurs in output spectrum. To minimize these spurs, dither is added to the system that reduces the spurs in output spectrum. Since, the DDFS is a digital system clock jitter also introduces noise in the output spectrum. Jitter is an abrupt and unwanted variation of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles. With advances in design and process technology, today's DDFS devices are very compact and draw little power (Bellaouar et al., 2000).

ARCHITECTURE

Phase locked loop

A phase locked loop is a closed loop control system which is used for the purpose of synchronization of the frequency and phase of a locally generated signal with that of an incoming signal. It is basically a nonlinear (the phase detector is a nonlinear device) feedback loop, as shown in Figure 1. The PLL consists of a voltage controlled oscillator (VCO), a phase detector, a variety of dividers, and a loop filter. The VCO is a device whose output frequency depends on the input control voltage. The relation is nonlinear but monotonic. However, when locked, the VCO can be assumed to be linear; it is both practical and convenient for analytical purposes.

Variation in the VCO control characteristics (that is, this nonlinearity) affects the loop parameters, and loop linearization (or compensation) is used extensively (Milan, 2003). Generally, the VCO output waveform is given by

$$A_{out} = A(v)\sin[\theta(t)+\varphi] \quad (1)$$

Where A is the signal amplitude and ω is the angular frequency, both depending on time *t*, and control voltage *v.* As a first approximation, A is assumed to have a constant envelope (does not depend on *t* or *v*) and that ω is a linear function of *v.*

Therefore Equation (1) can be written as

$$A_{out} = A \sin[\omega_0 + K_v v\ t]+\varphi \quad (2)$$

Here K_v is the VCO constant [rad/(Vs)]. Since we assume that the frequency is linearly dependent on *v* and is given by

$$\omega(v) = \omega_0 + K_v v \quad (3)$$

As mentioned, the linearization is justified and is assumed for the purpose of simpler analysis. In reality, when the loop is locked, frequency variations are tiny, and the constant-VCO assumption is correct as a piecewise linearization of the graph in Figure 1. Since phase is the integral of the angular frequency, the approximation can be completed by writing that the VCO transfer function, given by

$$\frac{\varphi_0(s)}{V} = \frac{K_v}{s} \quad (4)$$

As the Laplace transfer function of the VCO output phase. The phase detector produces an output voltage proportional to the difference in phase between its inputs and is always a nonlinear function. Typical phase

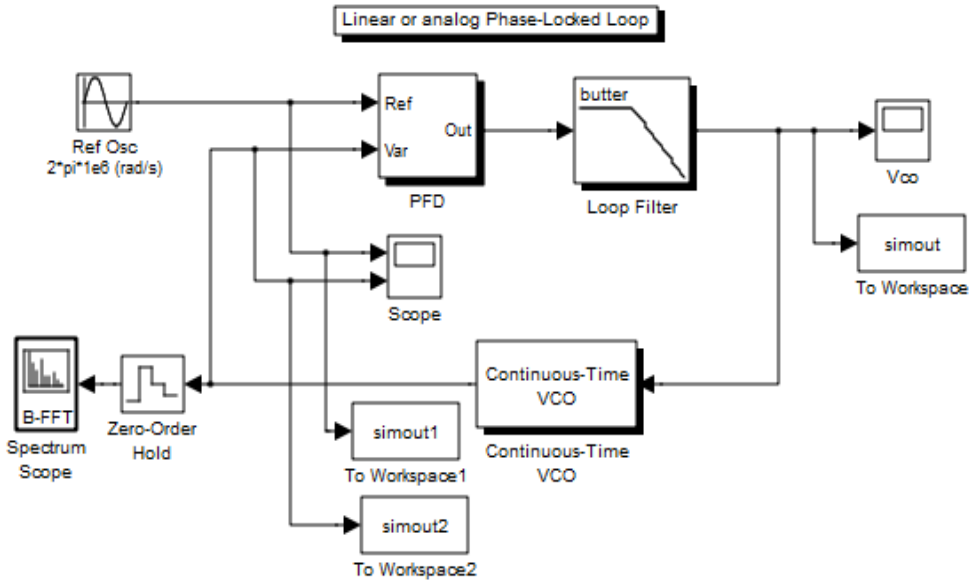


Figure 2. Simulink model of linear or analog PLL.

detector output voltage is given Equation (6). However, close to the locked position this function can be assumed to be linear (this is also justified since in the locked condition most frequency synthesizers operate with a very high signal-to-noise ratio and the phase detector therefore operates mainly at a fixed-phase position). Hence

$$V_d = K_d (\varphi_i - \varphi_0) \text{ V/rad} \quad (5)$$

Where V_d is the phase detector output voltage. Now the loop transfer functions can be described as

$$V_d = K_d (\varphi_i(s) - \varphi_o(s)) \text{ V/rad} \quad (6)$$

Let $V_c = V_d(s) F(s)$ be the control voltage

Where $F(s)$ is the loop filter transfer function and V_c is the VCO control voltage. Solving these simple equations yields

$$\varphi_0(s) = \frac{\varphi_i(s) K_d K_v F(s)}{s + K_v K_d F(s)} \quad (7)$$

and the transfer function H(s)= $\varphi_o(s)/ \varphi_i(s)$ is given by

$$H(s) = \frac{K_d K_v F(s)}{s + K_v K_d F(s)} \quad (8)$$

Also, following these equations will show that the error transfer function, defined as

$$H_e(s) = \frac{\varphi_i(s) - \varphi_o(s)}{\varphi_i(s)} \quad (9)$$

is given by

$$H_e(s) = \frac{s}{s + K_d K_v F(s)} \quad (10)$$

Since we linearized all components, given K_v and K_d, the feedback loop behavior depends mainly on $F(s)$. Also note that the error function has high-pass characteristics, and therefore a true direct-current (dc) modulation of a PLL circuit is not possible. This function, however, also referred to as dc frequency modulation, is possible in other synthesis techniques (Roland, 1999).

PLL based different frequency synthesizer

In this section, the different PLL models for frequency synthesis are discussed. Basically, in this research, five models of different PLL in MATLAB's SIMULINK toolbox were designed. Each model has its own advantages and limitations. So we cannot say that a particular model is used universally for all type of applications (Walters and Troudet, 1989).

Linear or analog PLL

The Simulink model of linear or analog PLL is shown in Figure 2.

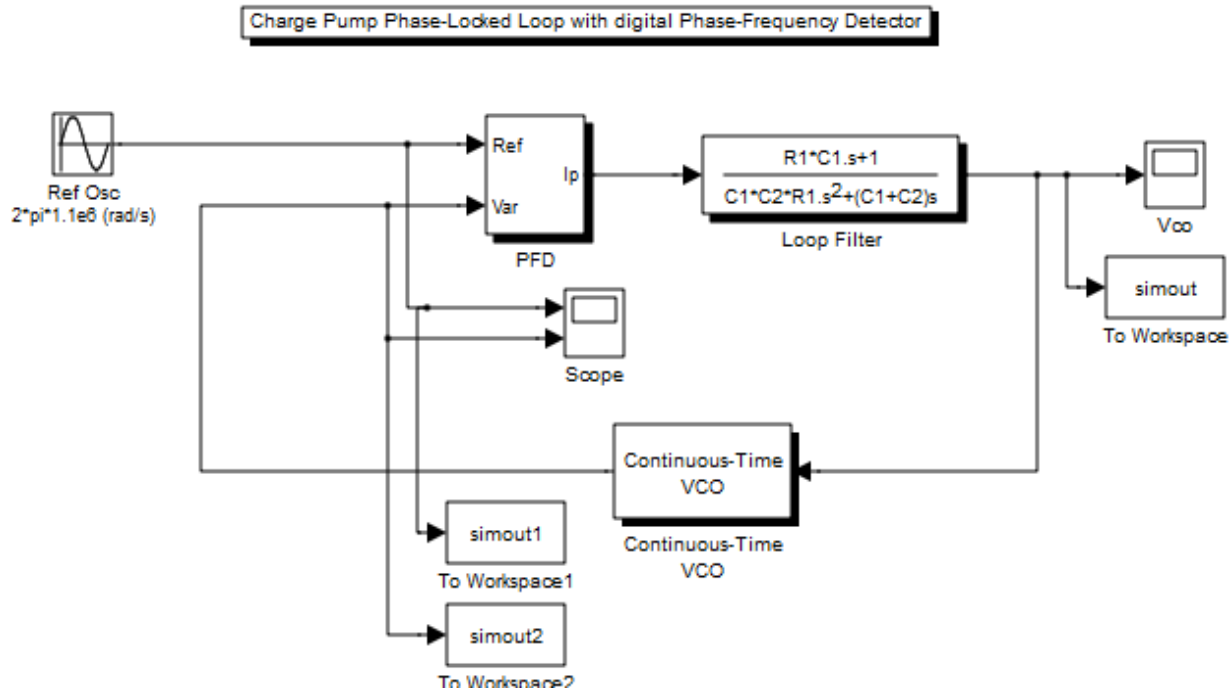


Figure 3. Charge pump phase.

Charge Pump PLL

The charge pump phase; Locked loop with digital phase frequency detector is shown in Figures 3. Power phase locked loop is shown in Figures 4a. Sub models of power phase locked loop are shown in Figures 4b and 4c.

Digital PLL

Digital PLL and sub model of digital PLL are shown in Figure 5a and 5b.

All digital PLL

All digital PLL and sub model of all digital PLL are shown in Figure 6a and 6b.

DDS COMPONENTS

Phase accumulator, which is controlled by Clock fs, is accumulated by step length K. N bit binary code, which is the output of phase accumulator, is seen as the address of ROM wave and addressing ROM. Amplitude code, which is the output of ROM, via D/A converter turns into step wave, then be smoothed by low pass filter, and complex signal waves, which is decided by amplitude code stored in ROM, can be gained finally. Thus, any waves can be generated by DDS. The process of wave generating is: ROM stores wave data, via every count value of address counter, corresponding to a location address of wave storage, circularly reads data of every location in turn, then send it to D/A converter, which convert it into corresponding analog quantity of output voltage, and ultimately be filtered by low pass filter generating smooth waves.

In the Figure 7, K means frequency control word; fs means clock frequency, N means the word length of phase accumulator, D means ROM data bit and the word length of D/A converter (James, 1994).

Frequency tuning equation

A sine wave is generally expressed as $x(t) = \sin(\omega t)$ which is non-linear and not easy to generate. The angular rate is given by $\omega = 2\pi f$ where, ω is the angular frequency. For an n-bit accumulator the output signal will have the frequency specified (Jouko, 2007).

$$f_{out} = \frac{\Delta p * f_{clk}}{2^n} \quad (11)$$

The phase rotation for that period can be determined by

$$\Delta p = \omega * \Delta t \quad (12)$$

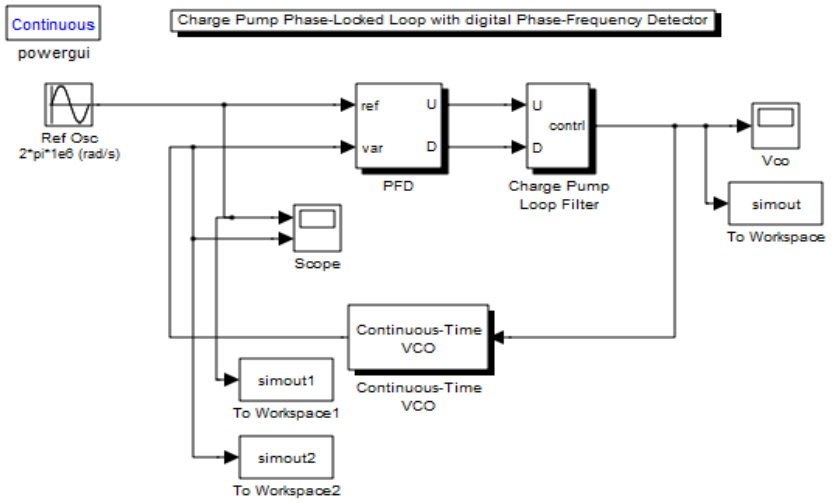
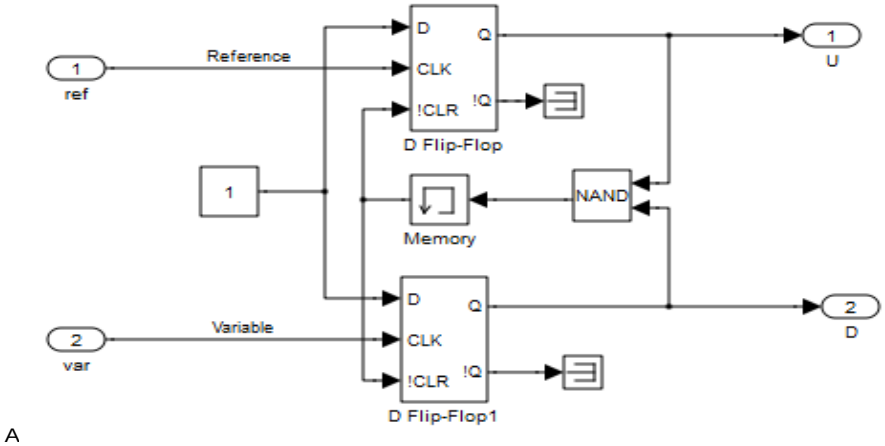
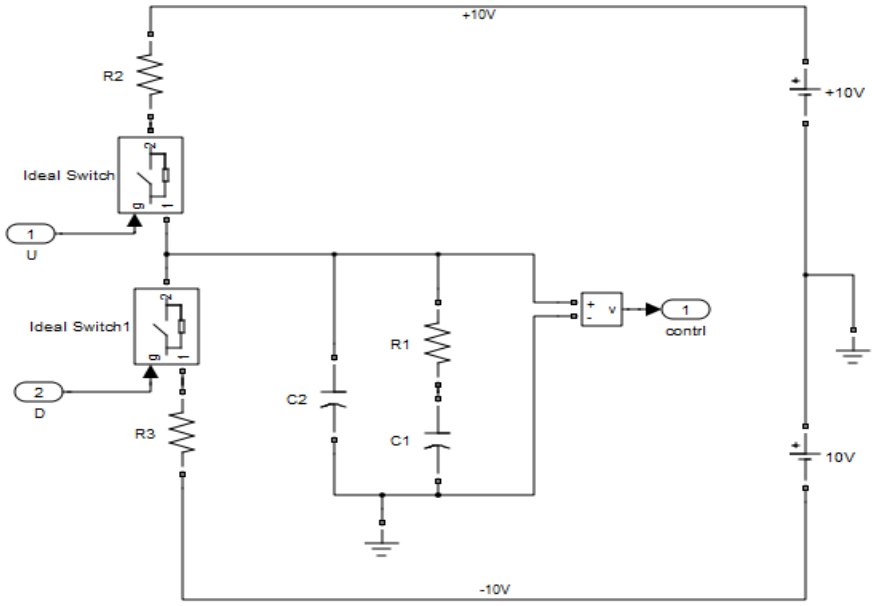


Figure 4a. Power phase locked loop.



A



B

Figure 4b and c. Sub models of power phase locked loop.

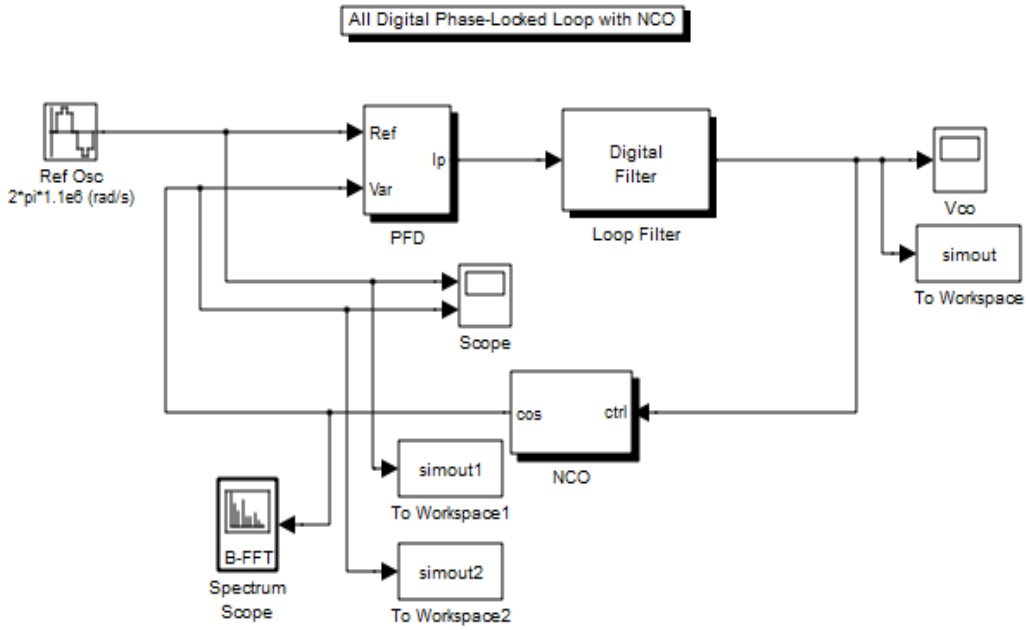


Figure 5a. Digital PLL.

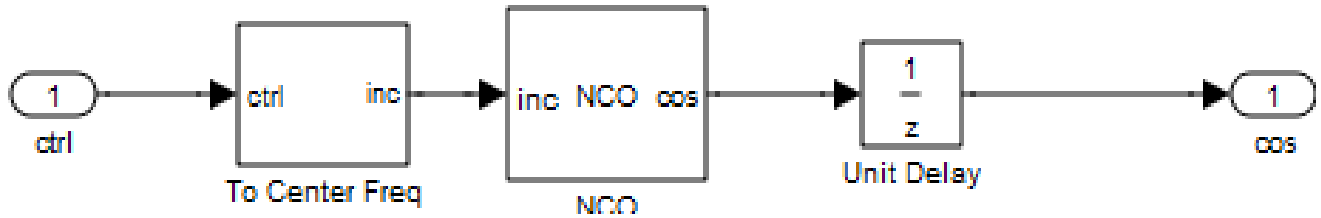


Figure 5b. Sub model of digital PLL.

Phase accumulator

Continuous-time sinusoidal signals have a repetitive angular phase range of 0 to 360°. The counter's carry function allows the phase accumulator to act as a phase wheel in the DDFS implementation. The PA is a modulo-M counter that increments its stored number each times it receives a clock pulse. The number of discrete phase points contained in the p wheel is determined by the resolution of the PA (n-bits), which determines the tuning resolution of the DDFS. The basic tuning equation for DDFS architecture

$$f_{out} = \frac{M * f_{clk}}{2^n} \quad (13)$$

with no phase and amplitude quantization, the output sequence of the look up table is given by,

Where: f_{out} = Output frequency of the DDS; M = Frequency control word; f_{clk} = System clock; n = Length of the phase accumulator (in bits).

Any change to the value of *M* results in immediate and phase-continuous changes in the output frequency (Martin et al., 2000).

Phase-to-Amplitude converter (ROM/ LUT)

In this study, the DDFS's ROM is a sine Look up Table; it converts digital phase input from the accumulator to output amplitude. The accumulator output represents the phase of the wave as well as an address to a word, which is the corresponding amplitude of the phase in the LUT.

This phase amplitude from the ROM LUT drives the DAC to provide an analog output. It is also called a digital Phase-to-Amplitude converter (PAC). In an ideal case

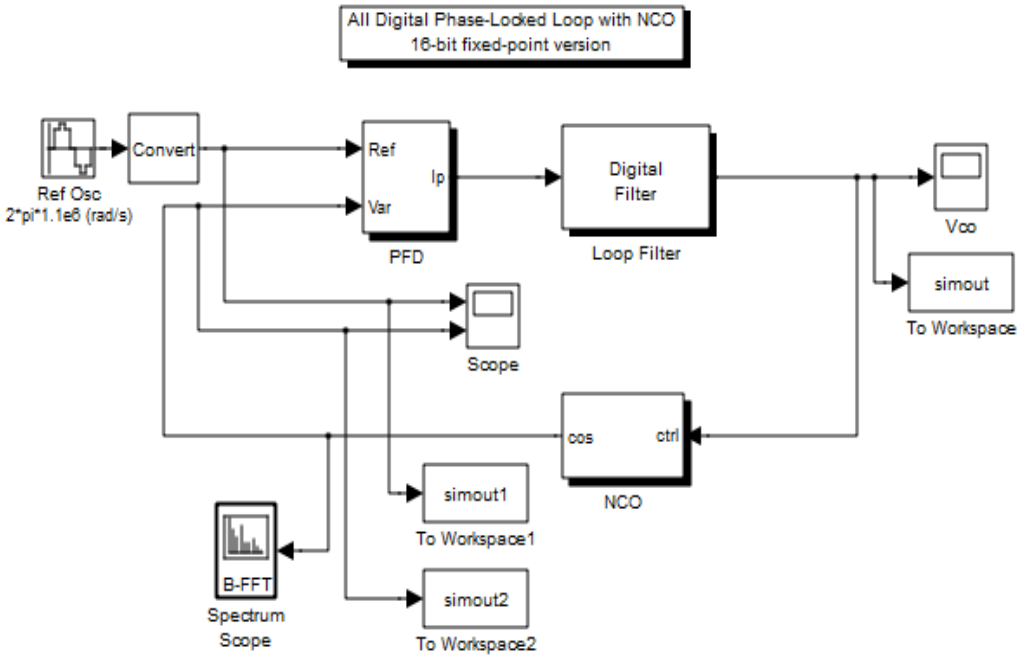


Figure 6a. All digital PLL.

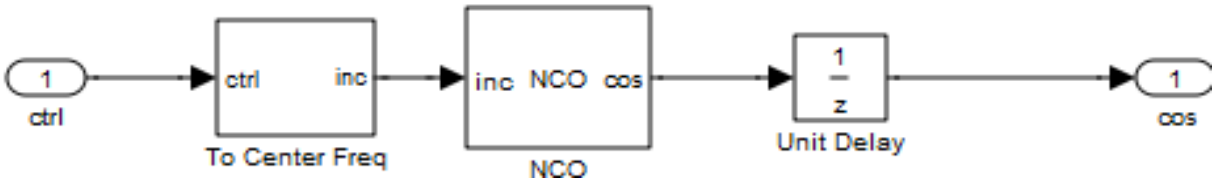


Figure 6b. Sub model of all digital PLL.

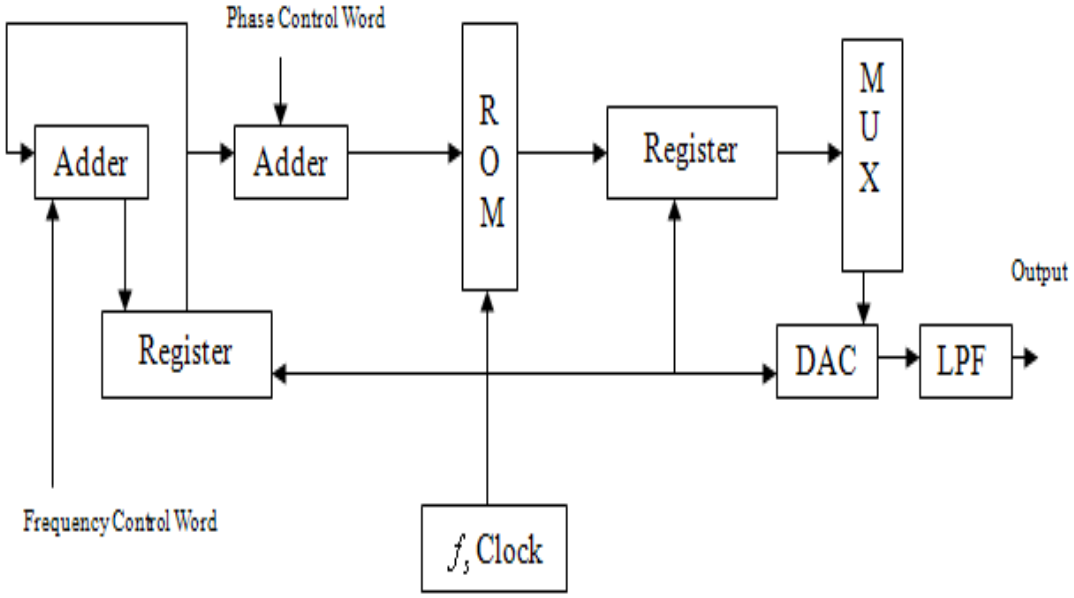


Figure 7. Block diagram of DDS.

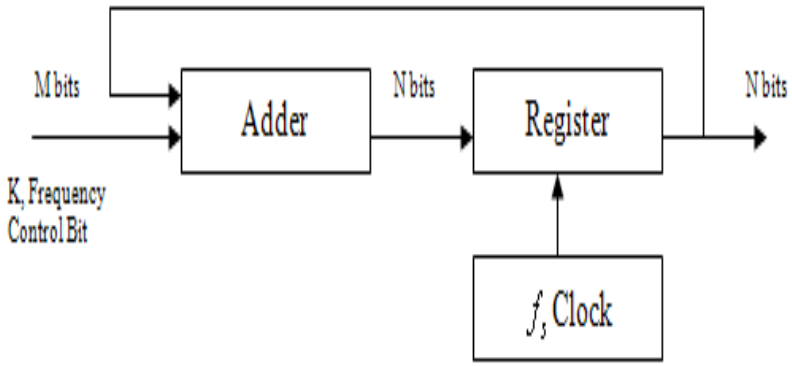


Figure 8. Phase accumulator.

$$\sin\left(\frac{2\pi * P(i)}{2^n}\right) \quad (14)$$

Digital-to-Analog converter and filter

The phase accumulator computes a phase (angle) address for the look-up table, which outputs the digital value of amplitude-corresponding to the sine of that phase angle-to the DAC. The DAC, in turn, converts that number to a corresponding value of analog voltage or current. The DAC and rest of the system run at the same reference clock for synchronization (Wu and Song, 2007).

DDS – driven PLL frequency synthesizer architecture

The block diagram of the DDS-driven PLL frequency synthesizer is shown in Figure 8. The reference frequency of DDS, f_{ref}, is generated by a crystal oscillator. The output frequency of DDS, $f_{DDS,}$ is controlled by the frequency tuning words. The reference of the PLL is driven by the output of DDS, f_{DDS}. The output of VCO is controlled by the output of charge pump (CP) of PLL. The output signal of this frequency synthesizer is obtained by multiplying f_{vco}.

The PLL module has a dual-modulus prescaler that has the pulse swallow function. This enables the large division ratio. The dual-modulus prescaler make it possible for the frequency synthesizer to generate higher output frequency while the frequency resolution is improved. The equation for the VCO frequency is

$$f_{vco} = (BP + A) \bullet \frac{f_{DDS}}{R} \quad (15)$$

The frequency of DDS is controlled by the frequency tuning word K, and

$$f_{DDS} = \frac{K}{2^N} \ f_{CLK} \quad (16)$$

Where N is the phase accumulator resolution of DDS and f_{CLK} is the internal clock of DDS. Then equation (15) can be written as

$$f_{VCO} = \frac{(BP + A)}{R} \bullet \frac{K}{2^N} \bullet f_{CLK} \quad (17)$$

In the scheme shown in Figure 9, since DDS module has good frequency resolution, from (17) it can be seen that the output signal has a better frequency resolution than traditional scheme.

The output of DDS can be described as Since the output of VCO is phase locked to the DDS, the output frequency of VCO changes according to the change of DDS. The output frequency of VCO can be described as

$$f_{DDS} = \frac{(K + \Delta K \bullet t)}{2^N} \bullet f_{CLK} \quad (18)$$

Where ΔK is the changing rate of frequency tuning word K.

$$f_{VCO} = \frac{(BP + A)}{R} \bullet \frac{(K + \Delta K \bullet t)}{2^N} \quad (19)$$

SIMULATION AND RESULTS

In order to analyse and evaluate the performance of the frequency synthesizers, the frequency settling time and synthesized signal of PLL were analyzed. Detailed discussions of simulated results are given in this section for each PLL one by one.

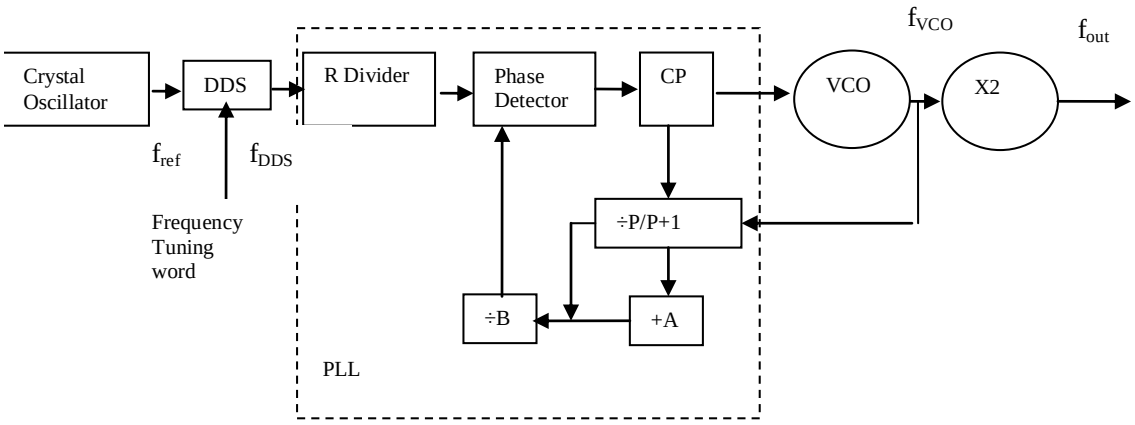


Figure 9. Block diagram of the DDS – driven PLL frequency synthesizer.

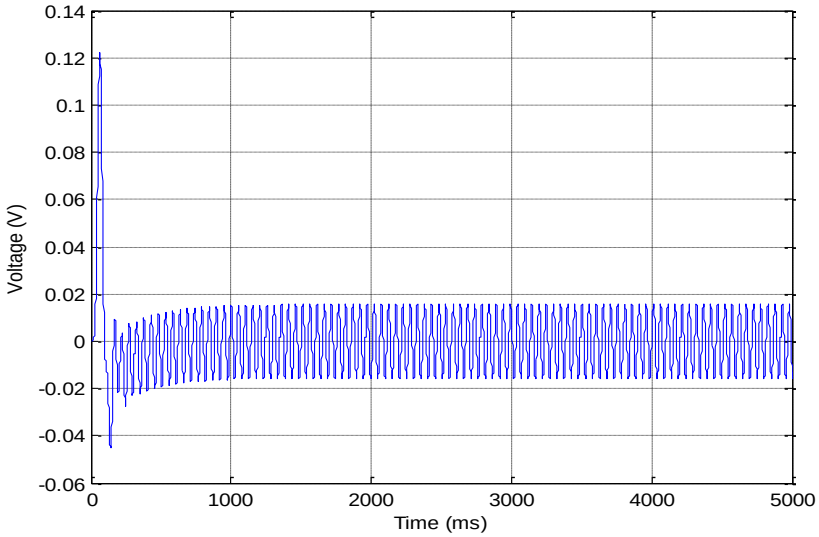


Figure 10. VCO output for linear or analog PLL.

Linear or Analog PLL

A classic or linear PLL uses a mixer as a phase detector. This yields a DC component that is proportional (but not linear) with the phase difference and a component at a frequency that is twice the input frequency. A loop filter isused to get rid of the second component. The output of the loop filter is fed into a VCO that increases the frequency if there is a positive phase difference and that decreases the frequency if there is a negative phase difference. Figures 10 and 11 shows the results of analog PLL.

Charge Pump PLL

Better results can be achieved with a charge pump and a loop filter. The charge pump, "pumps" current into a 2nd order loop filter. The branch voltage of the loop filter is used as input to the VCO. A digital phase frequency detector (PFD) determines whether a positive or negative current is pumped into the filter. Phase lead corresponds to a negative frequency (output and thus VCO frequency decreases) whereas phase lag corresponds to a positive current. Figures 12 and 13 show the results of CPLL.

The PFD is typically a finite state machine that responds to zero-crossings of the input signals. If the reference signal has a positive edge first a switch is turned on that pump a positive current into the loop filter, until a positive edge of the VCO signal is detected (phase lag). The simulation results of charge pump PLL and Power PLL are shown in the fig. In charge pump gain has been used as a charge pump and this gain is directly fed to transfer function which is a low pass filter. In power

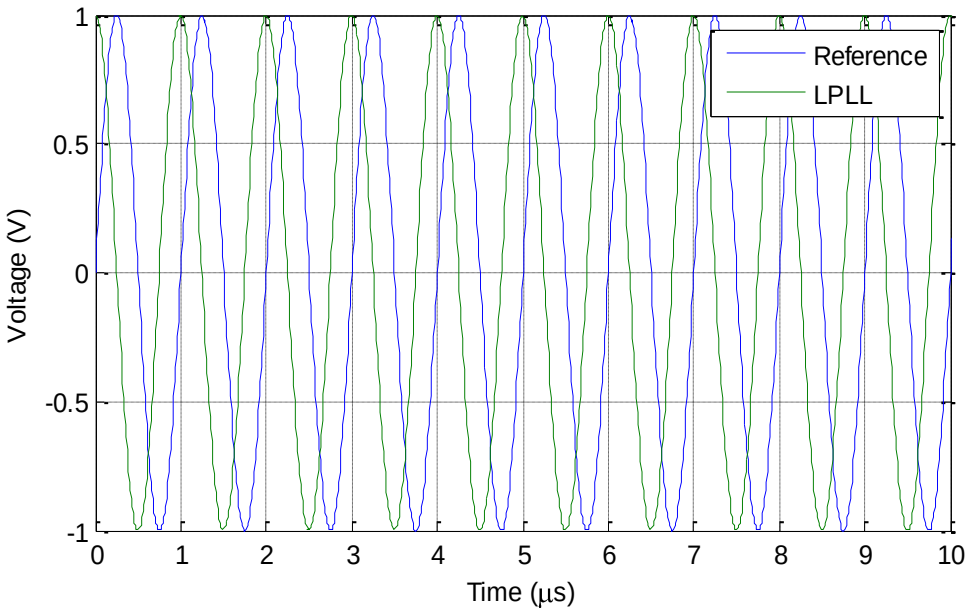


Figure 11. Output of linear PLL and reference signal.

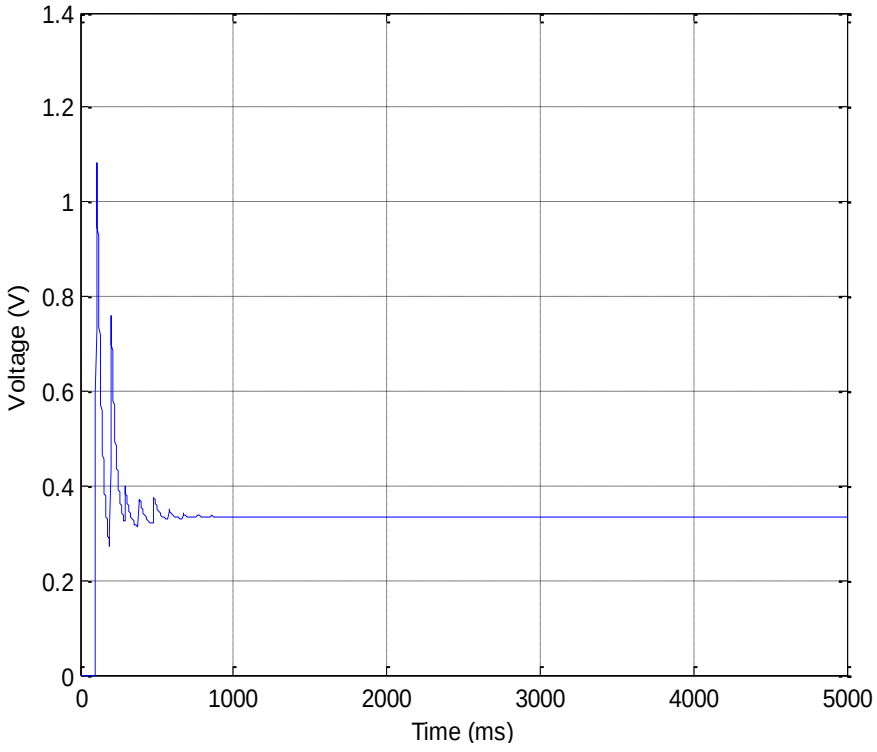


Figure 12. VCO output for charge pump PLL.

PLL, NAND gate is used as PFD. Simulation results shows that charge pump PLL and Power PLL settling time is nearly same (Bar-Giora, 1999). Figure 14 shows the result of PPLL.

Digital PLL

PLLs are used more and more in the digital domain, this means that apart for the Phase Frequency Detector, also

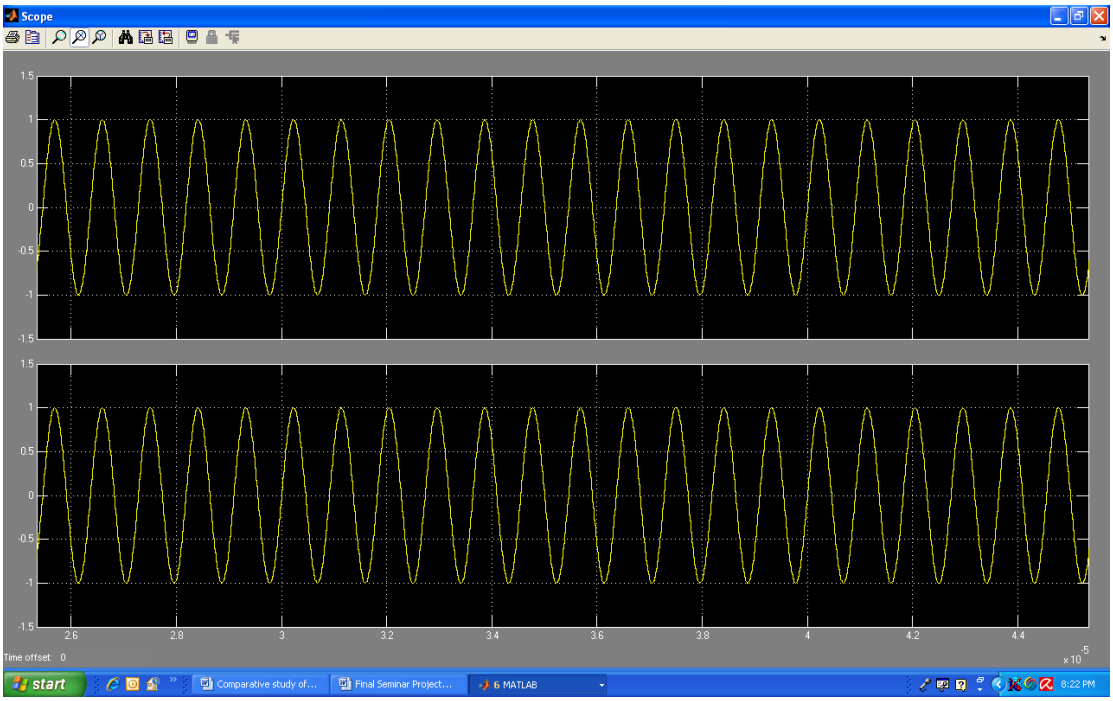


Figure 13. Output of CPLL and reference signal.

the loop filter and VCO need to be to be converted to discrete-time systems. The loop filter can be converted from Laplace to the z-domain using an appropriate transformation (e.g. Zero-Order Hold, Bilinear etc). The VCO (Voltage Controlled Oscillator) need to be replaced by an NCO (Numerically Controlled Oscillator). Figures 15 and 16 show the result of DPLL.

All Digital PLL

Many signal processing systems are implemented as hand-held devices (e.g. GPS, Mobile phones, multi-media) and need to be cost-effective. Therefore, it is often necessary to convert the system's data-types to fixed-point in order to implement the algorithm on either a fixed-point DSP, an FPGA or an ASIC (Application Specific Integrated Circuit). Figure 17 shows the result of All DPLL.

Phase noise

Since most applications require clean and precise clock signals, making a frequency synthesizer with low output phase noise is a major concern in this design. Because the PLL as part of the synthesizer system is an analog circuit, it is inherently sensitive to noise and interference. In particular, a ring oscillator, which is used in our VCO design, is the biggest phase noise. Other analog blocks including the charge pump and the loop filter also produce significant effects on the system in terms of phase noise. Therefore, a design with high supply and subtract noise rejection, such as one using differential circuit structure is desirable. In this research design, the differential VCO circuit topology and charge pump/loop filters were adopted.

Comparative analysis

Comparative analysis of all the PLLs is given in Table 1. 1 MHz reference signal for frequency synthesis was taken by using different PLLs. Some PLL gives much better and some of them give average performance for their particular frequency.

Simulation of DDFS with MATLAB

Matlab-Simulink implementation of a direct digital synthesizer consists of Phase Accumulator (PA) and Look up Table (LUT). The frequency of the output wave depends on the overflow rate of the PA and the frequency tuning word. This overflow rate depends on the frequency tuning word stored in the phase register. The overflow rate of the PA depends on the bit-size of the PA (number of bits) and the frequency tuning word. Larger the size of the frequency tuning word faster the PA overflows. To generate an output frequency of 10 MHz

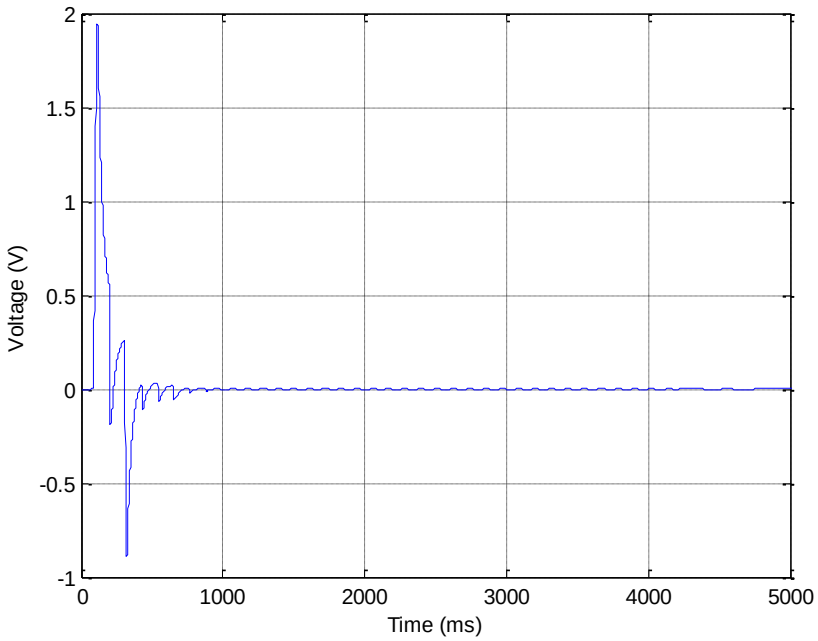


Figure 14. VCO output for power PLL.

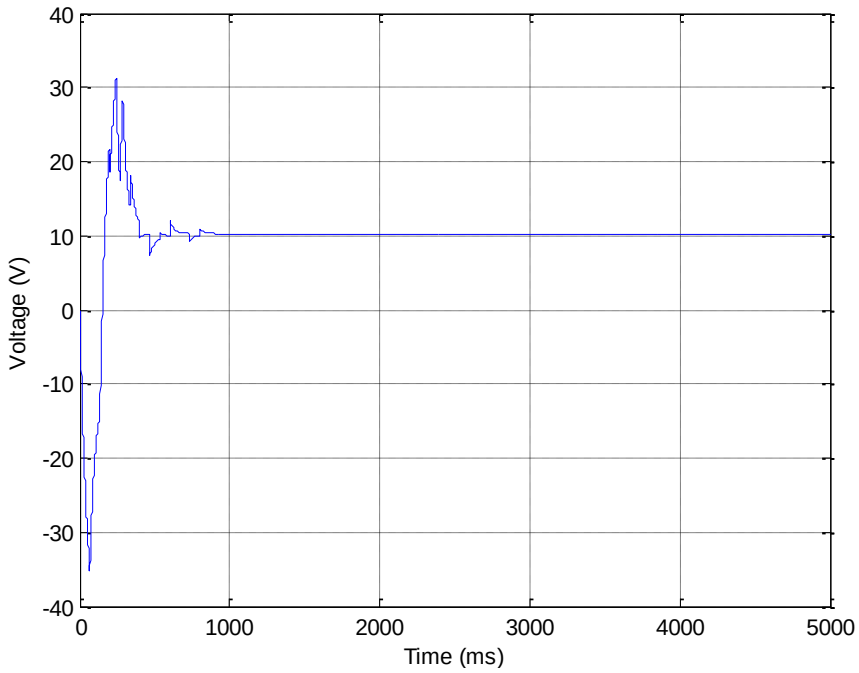


Figure 15. VCO output for digital PLL.

with a reference clock frequency of 50M Hz, a frequency tuning word (M) of 51 is stored in the Phase Register. The value of the frequency tuning word (M) is calculated using the frequency tuning equation. The Phase Accumulator is 8-bits wide. This control word M is added to the previous value of PA with each clock pulse. In the Figure 18, it can be seen that for a frequency tuning word of 51, for the first 3000 clocks, the PA overflows slightly more than two times (Dan, 2008). Therefore, the sine wave of lower frequency is produced, which is shown in Figure 19.

Alternatively, many industrial and biomedical applications

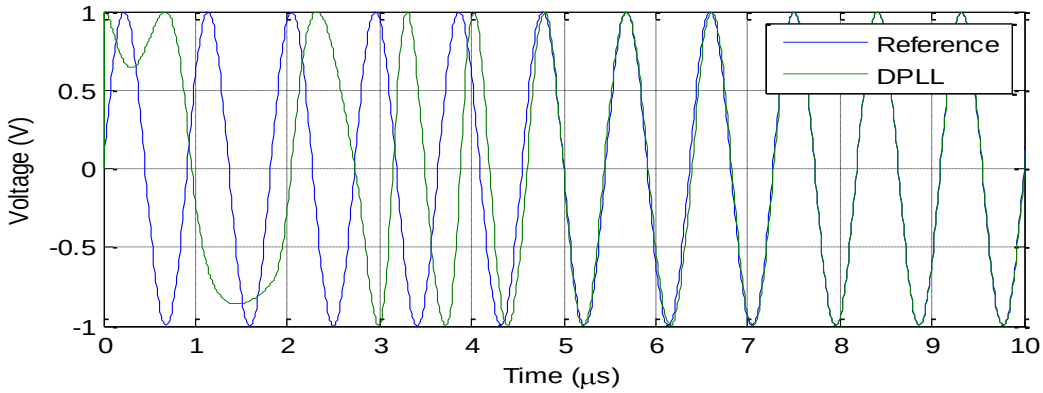


Figure 16. Output of digital PLL and reference signal.

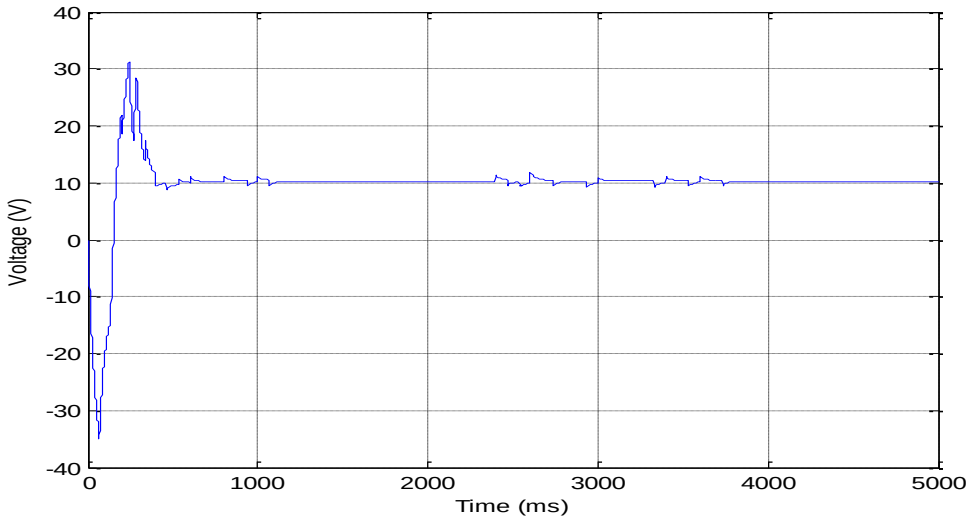


Figure 17. VCO output of All digital PLL.

Table 1. Comparative study of different PLLs.

PLLs	Linear or Analog PLL	Charge pump PLL	Power PLL	Digital PLL	All digital PLL
Settling time (s)	……..	6.0×10^{-6}	6.2×10^{-6}	8.5×10^{-6}	7.7×10^{-6}

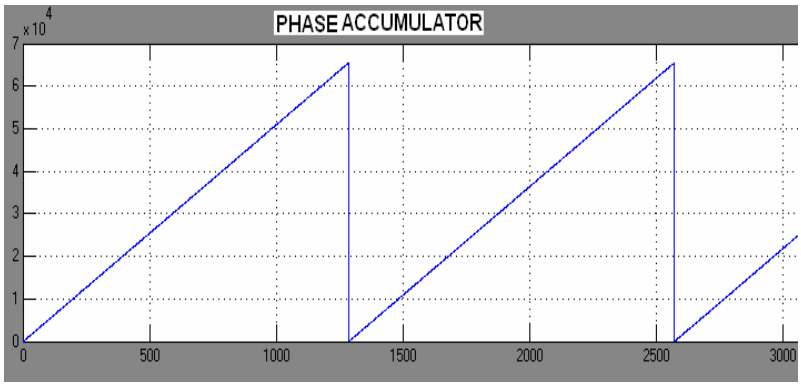


Figure 18. PA output for $M = 51$.

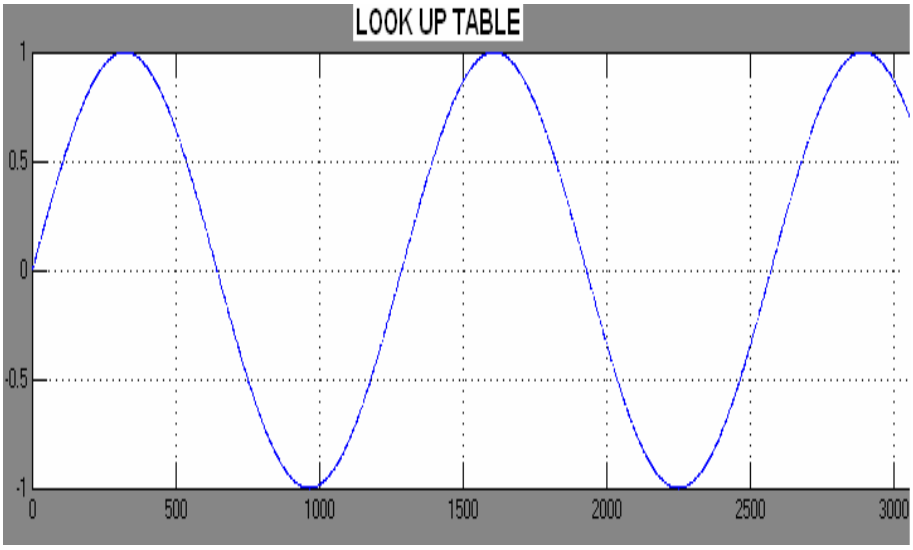


Figure 19. LUT output for = 10 MHz f*out.*

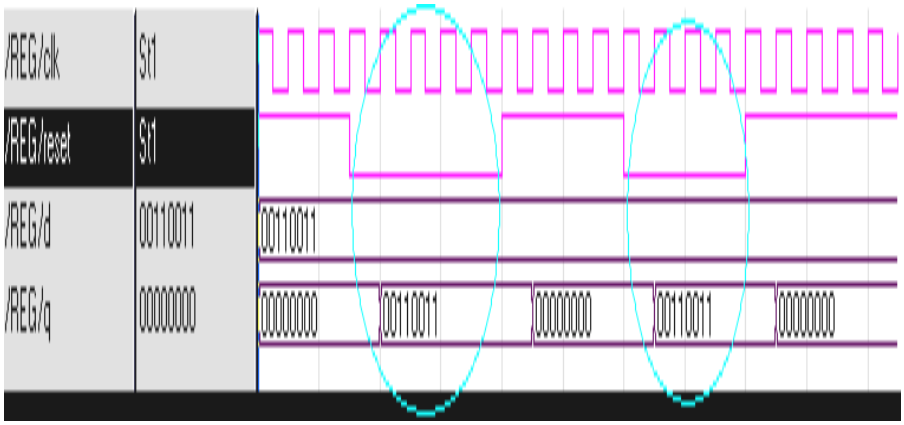


Figure 20. DDS output.

use a DDS as a programmable waveform generator. Because a DDS is digitally programmable, the phase and frequency of a waveform can be easily adjusted without the need to change the external components that would normally need to be changed when using traditional analog programmed waveform generator. It permits simple adjustments of frequency in real time to locate resonant frequencies on compensate for temperature drift.

DDFS simulation using ModelSim

This model has been implemented using VERILOG and simulated in ModelSim (YU and Zheng, 2005). This design consist of four basic modules, they are Top level, Register, Adder and the Look up Table (Figure 20).

CONCLUSION AND FUTURE SCOPE

In the first analysis, the simulated results of the different PLLs were shown. In the first simulation result, we see that phase frequency is not locked for 1 MHz signal or ittakes much time to lock the phase and frequency. In digital PLL, charge pump PLL gives better performance compared to power PLL, because in charge pump PLL gain is directly provided to transfer function of low pass filter, while it is not so for power PLL but the performance is almost the same. In ALL digital, the performance is not much better but this is a part of digital PLL and it is used for a specific purpose. So finally, we can say that each PLL have its own advantages and limitation according totheir use.In the second experiment results, it can be seenthat simulation and experiment are very consistent. Owing to the confine of hardware, only experiment

debugging of 8 bits frequency word can be done, so the frequency extent is relatively small. If debugging of 16 bits frequency word is done, the dynamic extent of frequency will be further improved. In this design Phase Accumulator's output is 8 bits, can but sample 256 points in one period, so the precision of synthesizing wave is not very high. If the output of Phase Accumulator is 10 bits, then 1024 points will be sampled in one period, the precision of the synthesizing wave will be improved very well. As the length of the phase accumulator increases, the size of the ROM/LUT increases exponentially. This reduces the speed of the DDFS and increases the size of hardware but more the number of bits in the phase accumulator, higher the frequency resolution. Therefore, there exists a trade off between size, frequency resolution and the speed. This issue of increase in the size of ROM can be solved with the phase truncation but that introduces noise in the output. The VERILOG modules, presented in this work are synthesizable on FPGA. The response of the DDFS mainly depends upon length of accumulator, desired output frequency and the clock frequency.

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