Review

Design of fast fault tolerant reversible signed multiplier

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Reversible logic circuits are emerging as a promising technology for power minimization. Parity preserving reversible circuits design will be very important for development of fault tolerant reversible systems in nanotechnology. In this paper, a fast fault tolerant reversible signed multiplier is proposed. In order to construct the multiplier, five variables parity preserving gate (F2PG) and modified new fault tolerant (MNFT) are designed, which are parity preserving reversible gates. The most significant aspect of F2PG is that it can work independently as a reversible fault tolerant full adder. Meanwhile, it can implement all Boolean functions. MNFT can reduce cross redundancy. The quantum implementations of F2PG and MNFT are also given. Otherwise, a new quantum implementation of the modified Islam gate (MIG) is presented. The Wallace tree is applied to improve the operating speed of the multiplier, which can implement the multiplication of two 5-bit binary signed numbers. Simulation and evaluation results indicate that the multiplier logic structure is correct with excellent performance.

Key words: Parity preserving reversible gate, fault tolerant, five variables parity preserving gate (F2PG), modified new fault tolerant (MNFT), reversible signed multiplier.

INTRODUCTION

Energy loss is an important consideration in digital design. R. Landaner showed that for irreversible logic computations, each bit of information loss generates KTln2 joules of energy, where K is Boltzmann's constant and T is the absolute temperature during computation (Landauer, 1961). Theoretically, a reversible logic circuit dissipates zero power since the input vector of reversible circuit can be uniquely recovered from the output vector. Bennett (1973) showed that zero energy would be possible if and only if the network consists of reversible gates. Consequently, reversibility will be an essential property of the future circuit designs.

Reversible computation is a promising study area with regard to the further technological advances. Applied in many applications, such as low power complementary metal-oxide-semiconductor (CMOS) design (Burr and Peterson, 1991), optical computing (Knil et al., 2001), DNA computing (Moore, 1998), quantum computing (Nielsen

and Chuang, 2002), thermodynamic, bioinformatics and nanotechnology (Merkle, 1993), it has received significant attentions in recent years. It is very clear that reversible computation will play a dominated role in future technologies.

A circuit (gate) is reversible if there is a one-to-one correspondence between the inputs and the outputs. Neither feedback nor fan-out is allowed (Perkowsi et al., 2001). In reversible logic design, an efficient design should minimize the followings (Islam et al., 2009):

Gate count: The number of gates used to realize the system.
Garbage outputs: The number of unused outputs in a reversible logic.
Constant inputs: The number of inputs kept constant at either 0 or 1.
Hardware complexity (Total logical calculation): The number of basic gates (NOT, AND and EX-OR gate) used to synthesize the given function.
Quantum cost: The cost of the circuit in terms of the cost of a primitive gate.

Fault tolerance is one property that the system still

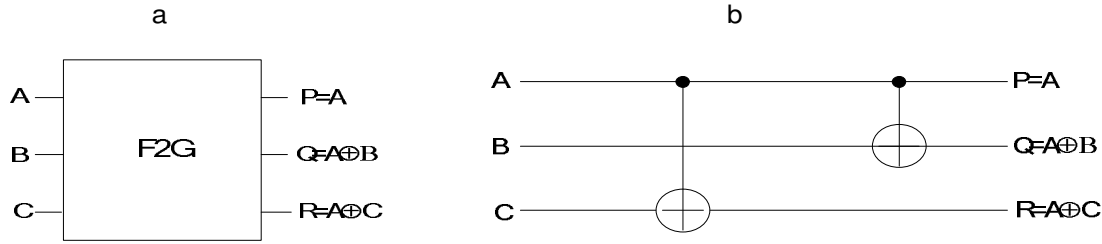*Corresponding author. E-mail: qxmyhyj@126.com. Tel: +86 0553-5910652.

Figure 1. 3×3 F2G gate: (a) symbol and functionality, (b) quantum equivalent representation.
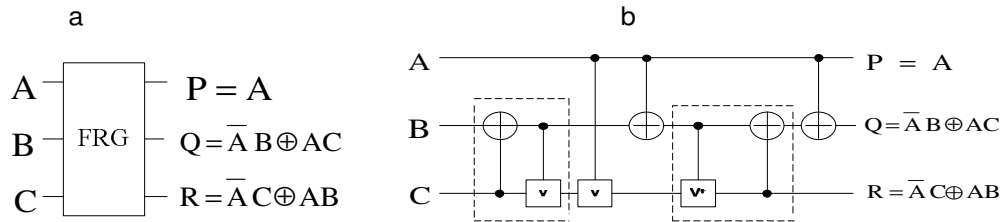

Figure 2. 3×3 FRG gate: (a) symbol and functionality, (b) quantum equivalent representation.

continues to use in operating properly even if some components fail. In communication and many other systems, fault tolerance is achieved by parity. Parity check is one of the widely used mechanisms for detecting single level fault. Thus, parity preserving reversible circuits design will be very important for the development of fault tolerant reversible systems in nanotechnology. A gating network will be parity preserving if its individual gate is parity preserving (Parhami, 2006; Islam and Begum, 2008). The synthesis of reversible logic circuit is significantly more complex than the conventional logic synthesis. It is also more difficult to make a fault tolerant reversible circuit than a conventional logic circuit. Therefore, it is necessary to search parity preserving reversible gates in order to construct parity preserving reversible circuits.

Multiplier circuits are of special importance because of the fact that they are the integral components of computer systems, cellular phones and most of the digital audio/ video devices, etc. There is one proposed reversible signed multiplier circuit in previous paper (Akbar et al., 2011). However, the available research results on fault tolerant reversible signed multiplier are very few. In this paper, two parity preserving reversible logic gates, five variables parity preserving gate (F2PG) and modified new fault tolerant (MNFT) are proposed. They can be used to design fault tolerant reversible logic circuits such as signed multiplier.

This paper is organized as follows: the brief introduction of the fault tolerant reversible logic gates required for the present work, new parity preserving reversible gates and their quantum implementation in detail, the description and simulation of fault tolerant signed multiplier and its evalua-tion. Finally, some conclusions and future work are depicted.

PARITY PRESERVING REVERSIBLE LOGIC GATES

Existing parity preserving reversible logic gates

Here, we review some parity preserving reversible logic gates which are used in this paper. For the convenience of calculating hardware complexity, we define the following parameters: α, a two input EX-OR gate calculation; β, a two input AND gate calculation; δ, a NOT calculation; TC, total logical calculation.

A reversible gate is called parity preserving reversible logic gate if its input parity matches the parity of its output. More formally, any K×K reversible logic gate where the EX-OR of the inputs matches the EX-OR of the outputs will be parity preserving (Islam and Begum, 2008). A few of the parity preserving reversible logic gates have been proposed in the literatures (Parhami, 2006; Fredkin and Toffoli, 1982; Hagpharast and Navi, 2008; Islam et al., 2009).

Feynman double gate

Figure 1 shows a 3×3 Feynman double gate (Parhami, 2006) (F2G). The quantum cost of a F2G gate is 2, and the total logical calculation TC is 2α.

Fredkin gate

Figure 2 shows a 3×3 Fredkin gate (Fredkin and Toffoli, 1982) (FRG). The quantum cost of a FRG gate is 5, and the total logical calculation TC is 2α+4β+2δ.
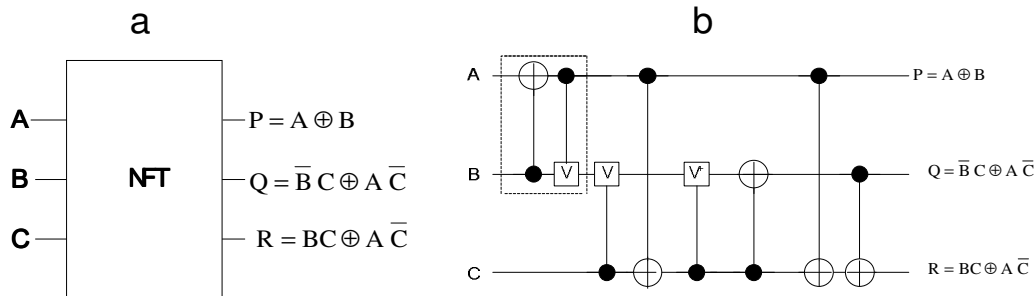
Figure 3. 3×3 NFT gate: (a) symbol and functionality, (b) quantum equivalent representation.
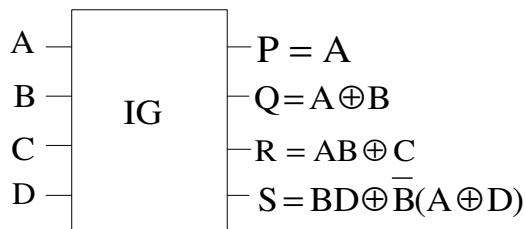

Figure 4. Symbol and functionality of 4×4 IG gate.

New fault tolerant gate

Figure 3a shows a 3×3 new fault tolerant gate (Hagpharast and Navi, 2008) (NFT). The quantum cost of a NFT gate is 5, while in our opinion; it is 7 as shown in Figure 3b. The total logical calculation TC is $4\alpha+3\beta+2\delta$.

Modified Islam gate

Figure 4 shows a 4×4 Islam gate (Islam and Begum, 2008) (IG). Figure 5a shows a 4×4 modified Islam gate (Islam et al., 2009) (MIG). The quantum implementation of MIG is designed in a new method as shown in Figure 5b. The quantum cost of a MIG gate is 7 because the quantum cost of a PG gate is 4 (Peres, 1985). Total logical calculation TC is $3\alpha+2\beta+\delta$. The quantum cost of an IG gate is also 7. Total logical calculation TC is $4\alpha+3\beta+\delta$.

New parity preserving reversible logic gates

New 5×5 parity preserving reversible logic gate

A 5×5 parity preserving reversible gate logic called F2PG is proposed and shown in Figure 6, its optimal quantum implementation by template matching and applying the moving rule (Miller et al., 2003) is revealed in Figure 7. The input vector is I (A, B, C, D and E) and the output vector is O (P, Q, R, S and T). The outputs are described as $P = AC \oplus B\overline{C} = (A \oplus B)C \oplus B$, $Q = A \oplus B$, $R = A \oplus B \oplus C$, $S = (A \oplus B)C \oplus AB \oplus D$ and $T = A\overline{B} \oplus E = AB \oplus A \oplus E$. The

optimized quantum cost of a F2PG gate is 14. Total logical calculation TC is $10\alpha+3\beta$. The corresponding truth table of the F2PG gate is as shown in Table 1. It can be verified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined. The F2PG gate is also parity preserving, owing to $A \oplus B \oplus C \oplus D \oplus E \leftrightarrow P \oplus Q \oplus R \oplus S \oplus T$. Therefore, F2PG gate is parity preserving reversible logic gate.

The F2PG gate can implement any Boolean functions, AND, OR, NOT, XOR, etc. Boolean functions can be obtained as depicted in Figure 8a to d. One of the most prominent features of F2PG gate is that it can work singly as a fault tolerant reversible full adder unit. The full adder using F2PG is acquired with D=0, E=0 and C=C_{in} as shown in Figure 9.

Modified new fault tolerant logic gate

In this paper, in order to decrease cross redundancy, the NFT gate (Hagpharast and Navi, 2008) is modified and called the MNFT gate as shown in Figure 10. The input vector is I (A, B and C) and the output vector is O (P, Q and R). The outputs are described as $P = A\overline{C} \oplus B C = (A \oplus B)C \oplus A$, $Q = A \oplus B$ and $R = A\overline{C} \oplus \overline{B} C = (A \oplus B)C \oplus A \oplus C$. The quantum cost of a MNFT gate is 5 as shown in Figure 11. Its total logical calculation TC is $5\alpha+\beta$. The corresponding truth table of the MNFT gate is as shown in Table 2. It can be verified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined. It is noted that the MNFT gate is parity preserving, because of $A \oplus B \oplus C \leftrightarrow P \oplus Q \oplus R$.

THE APPLICATION OF NEW PARITY PRESERVING REVERSIBLE LOGIC GATES

Fault tolerant adder circuit based on F2PG

Fault tolerant full adder circuit

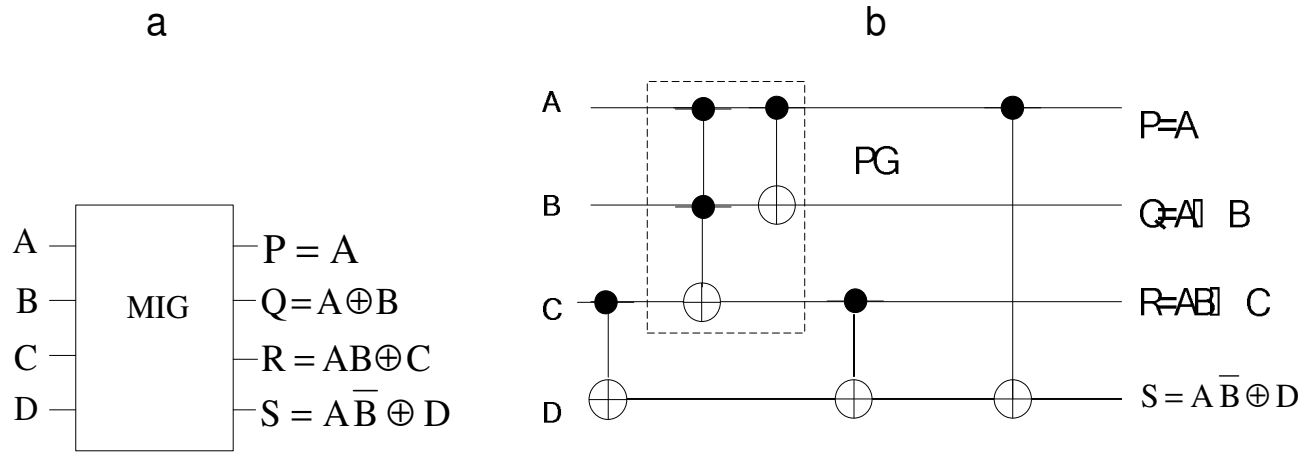Reversible logic implementation of fault tolerant full adder

a

b

A ──┤   ├── P = A

B ──┤ MIG ├── Q=A⊕B

C ──┤   ├── R = AB⊕C

D ──┤   ├── S = A$\overline{B}$ ⊕ D

P=A

Q=A⊕B

R=AB⊕C

S = A$\overline{B}$ ⊕ D

PG

Figure 5. 4×4 MIG gate: (a) symbol and functionality, (b) quantum equivalent representation.

Table 1. Truth table of the F2PG gate.

| A	B	C	D	E	P	Q	R	S	T
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	1	1	1	0	0
0	1	0	0	1	1	1	1	0	1
0	1	0	1	0	1	1	1	1	0
0	1	0	1	1	1	1	1	1	1
0	1	1	0	0	0	1	0	1	0
0	1	1	0	1	0	1	0	1	1
0	1	1	1	0	0	1	0	0	0
0	1	1	1	1	0	1	0	0	1
1	0	0	0	0	0	1	1	0	1
1	0	0	0	1	0	1	1	0	0
1	0	0	1	0	0	1	1	1	1
1	0	0	1	1	0	1	1	1	0
1	0	1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	0	1	0
1	0	1	1	0	1	1	0	0	1
1	0	1	1	1	1	1	0	0	0
1	1	0	0	0	1	0	0	1	0
1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	1	0	0	0	0
1	1	0	1	1	1	0	0	0	1
1	1	1	0	0	1	0	1	1	0
1	1	1	0	1	1	0	1	1	1
1	1	1	1	0	1	0	1	0	0
1	1	1	1	1	1	0	1	0	1
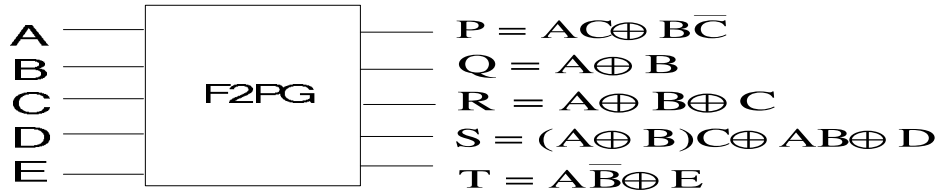
Figure 6. Symbol and functionality of 5×5 F2PG gate.
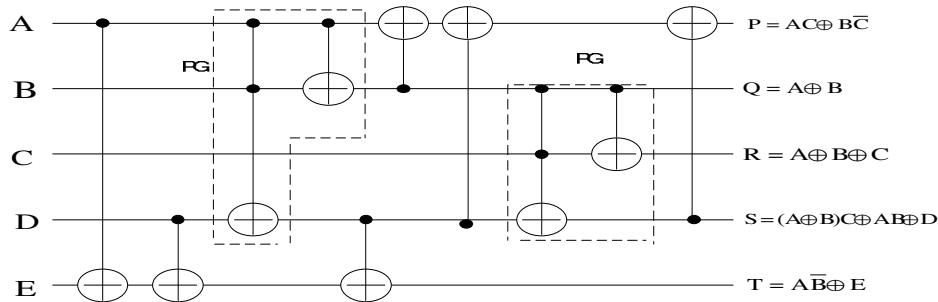

Figure 7. Quantum equivalent realization of 5×5 F2PG gate.
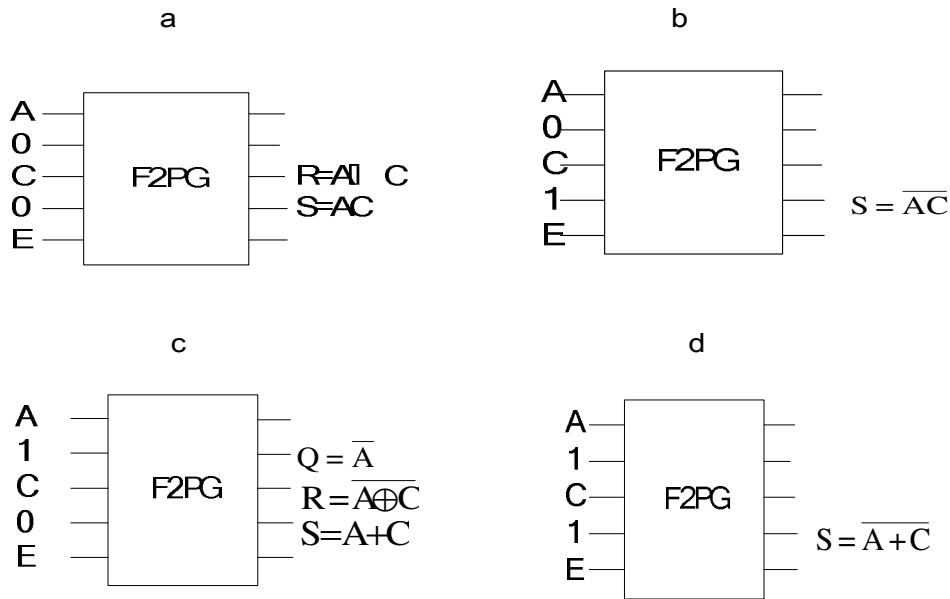
a

b

c

d

Figure 8. Boolean functions of 5×5 F2PG gate: (a) XOR and AND, (b) NAND (c) NOT, NXOR and OR, (d) NOR.

circuit has been studied (Islam and Begum, 2008; Islam et al., 2009; Haghparast and Navi, 2008; Bruce et al., 2002). It has been proved (Islam and Begum, 2008) that any realization of a fault tolerant reversible full adder circuit needs at least three garbage outputs and two constant inputs. The circuit requires six parity preserving reversible

gates (two FRGs and four F2Gs) (Haghparast and Navi, 2008) and four FRGs (Bruce et al., 2002). The rest uses two IGs (Islam and Begum, 2008) and two MIGs (Islam et al., 2009), respectively. This paper presents a new design of fault tolerant reversible full adder circuit that uses only one F2PG, which is described in Figure 9.
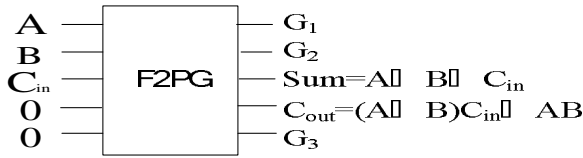
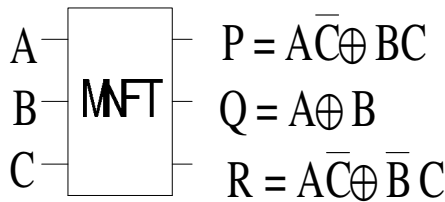**Figure 9.** F2PG gate as reversible fault tolerant full adder.

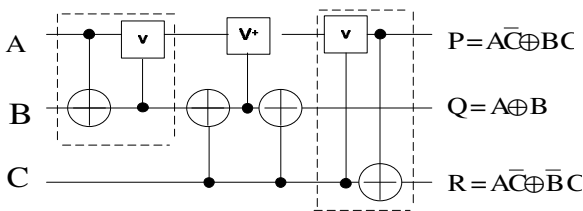**Figure 10.** Symbol and functionality of MNFT gate.

Figure 11. Quantum equivalent realization of MNFT gate.

Table 2. Truth table of the MNFT gate.

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	1	1	0
1	0	0	1	1	1
1	0	1	0	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Evaluation of the proposed fault tolerant full adder circuit

The designed fault tolerant reversible full adder circuit is more efficient than the existing presented (Islam and Begum, 2008; Islam et al., 2009; Haghparast and Navi, 2008; Bruce et al., 2002). Evaluation can be compre-hended easily with the help of the comparative results from Table 3. The proposed circuit needs only one gate and its quantum cost is 14, and constant inputs and garbage outputs are two and three respectively, while

these are the minimum theoretically. So far, the best circuit is two gates, and the quantum cost is 14 (Islam MS, Begum, 2008; Islam et al., 2009). Hence, the designed circuit in the present study is better than all the existing counterparts.

In the digital signal processing, the speed of multiplier has played an important role in the performances of chips and systems. Generally, the speed of multiplier depends on the algorithm and structure. It can be implemented in shift-add algorithm, Pezaris algorithm or Baugh-Wooley algorithm (Baugh and Wooley, 1973; Ma GK and Taylor, 1990). The shift-add algorithm is based on the unsigned number, and has some deficiencies such as long delay and low speed. It is unsuitable for very-large-scale integration (VLSI). Pezaris and Baugh-Wooley algorithms can be directly used in the complement multiplier, improving the speed of multiplier. However, because heterogeneous full-adders have irregular multiplication rules used in the Pezaris algorithm, it is of no benefit in designing the layout of VLSI. Hence, a reversible signed multiplier based on Baugh-Wooley algorithm is adopted. It only needs one kind of full adder which requires supplements, which can be achieved by MNFT gate. As a result of the low quantum cost of MNFT, the designed multiplier can save time and promote the speed of operation.

In this paper, the multiplication is implemented in the form of the modified Baugh-Wooley method (Akbar et al., 2011). Fault tolerant reversible signed multiplier circuits have two parts. First, the partial products are generated in parallel. Second, multi-operand addition is performed in Wallace tree method. The operation of 5×5 multiplier is depicted in Figure 12. It consists of 25 partial product bits of the form $x_i y_j$ (i=0,1,…4, j=0,1,…4).

Fault tolerant reversible signed multiplier based on F2PG and MNFT

Fault tolerant reversible partial product generation circuit

To perform AND and NAND gates, the FRG gate and the MNFT gate are applied. At the meantime, we make use of cascaded gates and "Copying circuit" (e.g. F2G) to increase the fan-out. So, output signals of one gate can be inputs of the other gates. The reversible fault tolerant partial products can be generated in parallel as shown in Figure 13.

Fault tolerant reversible signed multiplier based on F2PG gate and Wallace tree

In the signed multiplier, a Wallace tree structure is used for implementing one time of addition for n operands. In order to reduce the carry transfer delay of partial product in adder array of the multiplier, it is necessary to design

Table 3. Comparative results of different fault tolerant full adder circuits.

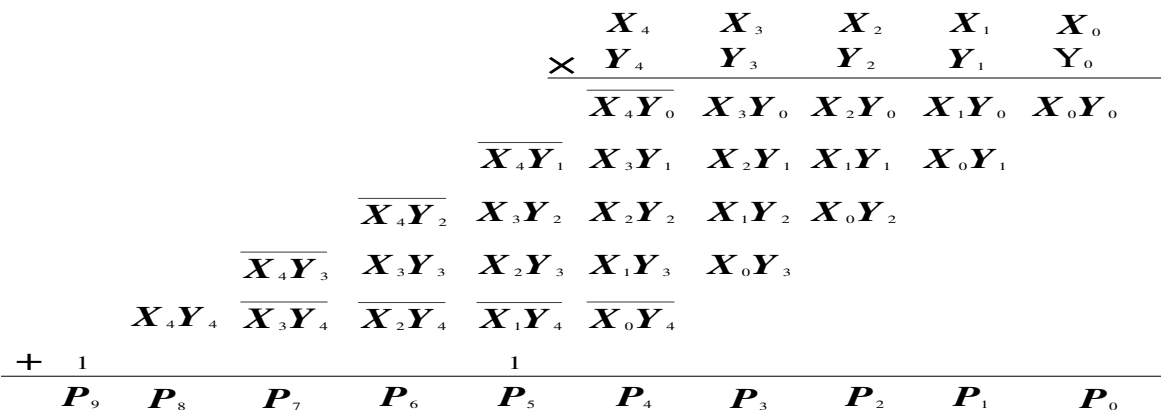|	Gate count	Constant inputs	Garbage outputs	Total quantum cost	Total logical calculation
Islam and Begum (2008)	2 (2=2IGs)	2	3	14	$8\alpha+6\beta+2\delta$
Islam et al. (2009)	2 (2=2MIGs)	2	3	14	$6\alpha+4\beta+2\delta$
Haghparast and Navi (2008)	6 (6=2FRGs+4F2Gs)	5	6	18	$12\alpha+8\beta+4\delta$
Bruce et al. (2002)	4 (4=4FRGs)	2	3	20	$8\alpha+16\beta+8\delta$
Proposed	1 (1=1F2PG)	2	3	14	$10\alpha+3\beta$

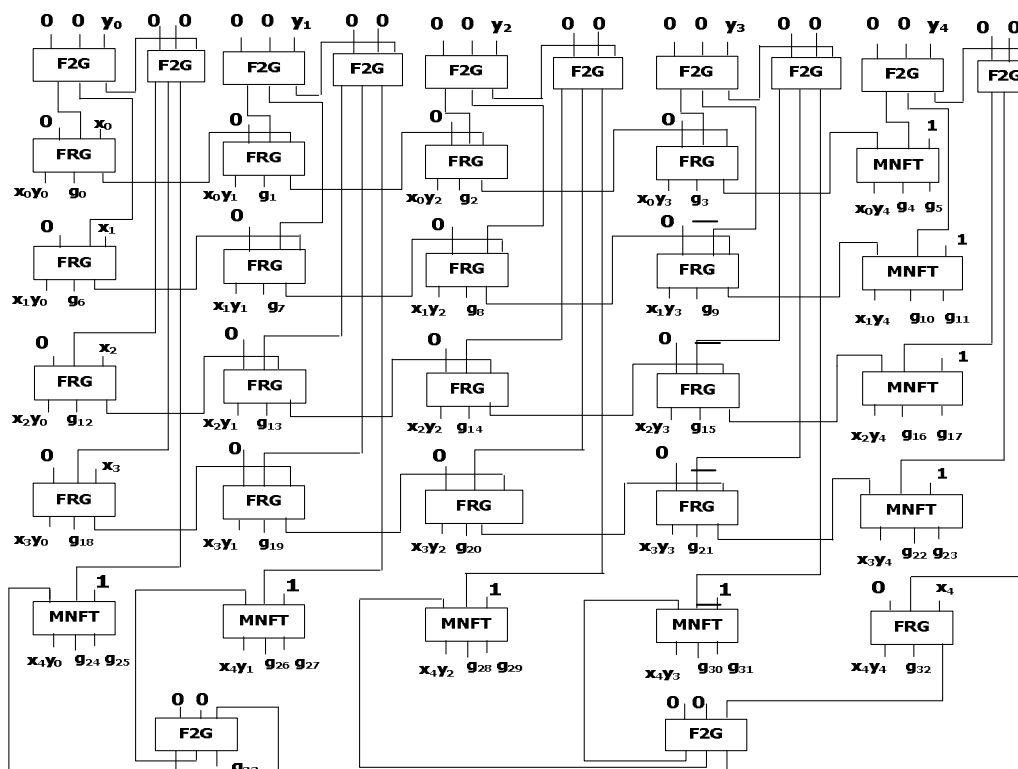**Figure 12.** 5×5 Signed multiplier by modified Baugh-Wooley.

Figure 13. 5×5 fault tolerant reversible partial products generation circuit.
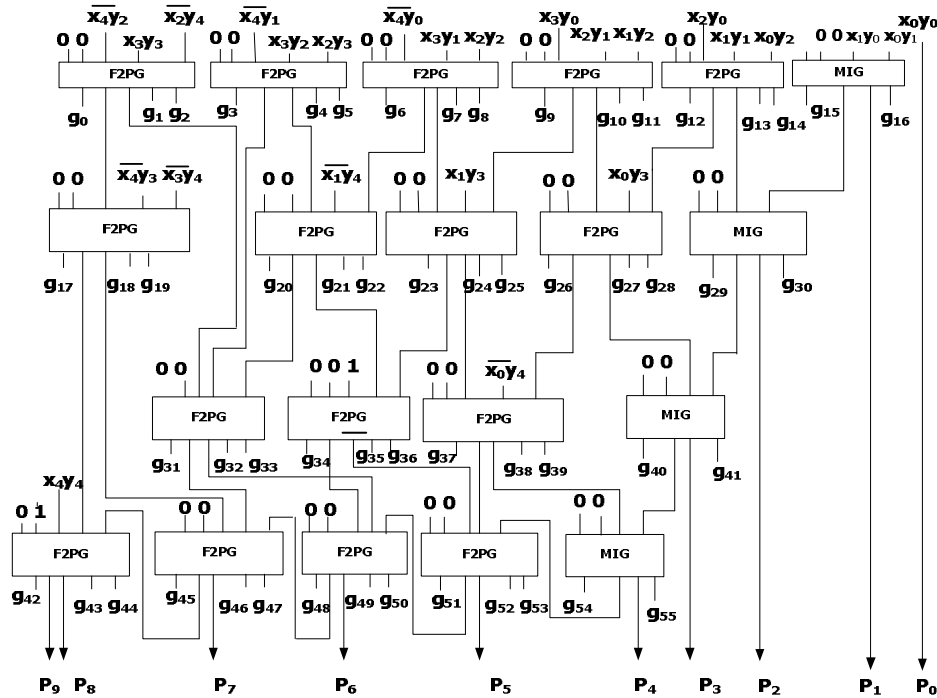
Figure 14. Circuit of 5×5 fault tolerant reversible signed multiplier.
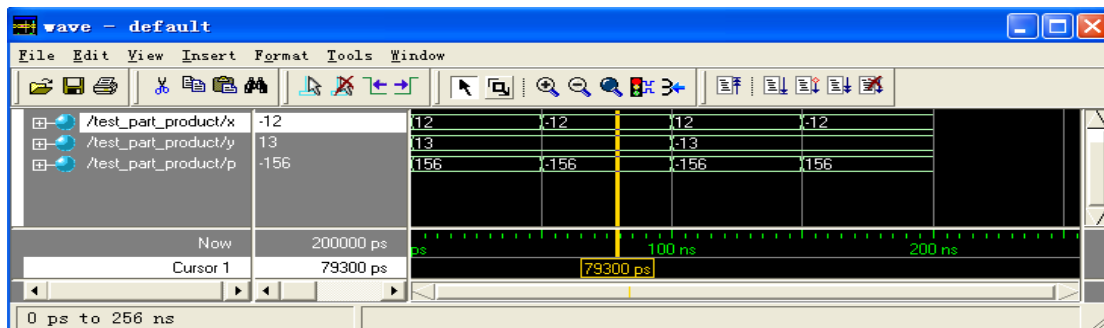

Figure 15. The result of signed multiplier's function simulation.

its Wallace tree. In other words, it improves the operating speed in the whole adder array. Different from the design of ripple carry adder array, in the Wallace tree, those bits with the same weight in the corresponding partial products are added together, rather than one by one. Usually, the full adder is used to accomplish the addition of bits with the same weight. While in this paper, one bit full adder is applied. In the per layer of Wallace tree, the number of the partial product vectors can be decreased according to the proportion of 3-2, e.g., every 3 figures produce one sum bit and one carry bit. The whole array delay is reduced from O (n×n) to O (n×log(n)). The 5×5 fault tolerant signed multiplier is as shown in Figure14 using a F2PG gate as a reversible full adder and a MIG gate as a half adder. It is also possible to use a F2PG

gate as a half adder as mentioned earlier in this study, where it needs less hardware complexity and quantum cost in the reversible half adder with a MIG gate, e.g. the quantum cost of a MIG gate is 7, whereas for F2PG it is 14.

Fault tolerant reversible signed multiplier's function simulation

When two complement operands are encoded in Verilog hardware description language (HDL), 1 bit for sign, 4 bits for value, the Wallace tree is applied in the summation of the partial products. As shown in Figure 15, in the simulation of the signed multiplier, the operands are

Table 4. Characteristics of 5×5 fault tolerant reversible partial product generation circuit.

Gate count	Constant inputs	Garbage outputs	Total quantum cost	Total logical calculation
37*	49	34	149	98α+76β+34δ

*MNFT: 8, FRG: 17. F2G, 12

Table 5. Characteristics of 5×5 fault tolerant reversible signed multiplier circuit.

Gate count	Constant inputs	Garbage outputs	Total quantum cost	Total logical calculation
57*	90	90	401	270α+132β+38δ

*MNFT: 8, FRG: 17, F2G: 12, F2PG: 16, MIG: 4.

expressed in decimal form. Its correctness is indicated in the four test cases, such as 12×13, -12×13, 12×(-13) and -12×(-13).

EVALUATION OF THE DESIGNED FAULT TOLERANT REVERSIBLE SIGNED MULTIPLIER CIRCUIT

After fault tolerant reversible signed multiplier circuit is designed, the evaluation can be comprehended easily with the help of the results from Tables 4 and 5. The quantum cost of a F2PG is 14. The quantum cost of MIG, F2G, FRG and MNFT is equal to 7, 2 (Parhami, 2006), 5 (Fredkin and Toffoli, 1982) and 5, respectively. Total logical calculation TC of F2PG, MIG, F2G, FRG and MNFT is 10α+3β, 3α+2β+δ, 2α, 2α+4β+2δ and 5α+β, respectively.

Table 4 gives the characteristics of 5×5 fault tolerant reversible partial product generation of the circuit. Table 5 gives the characteristics of 5×5 fault tolerant reversible signed multiplier of circuit.

CONCLUSIONS AND FUTURE WORK

In this paper, the fault tolerant reversible signed multiplier is composed of two kinds of new reversible logic gates, such as F2PG and MNFT, whose hardware complexity and quantum implementation are presented. The quantum cost of the 5*5 multiplier that is composed of 57 gates is 401. In future works, it is necessary to study the optimization of fault tolerant reversible gate network.

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