International Journal of the Physical Sciences Vol. 6(10), pp. 2372-2379, 18 May, 2011
Available online at http://www.academicjournals.org/IJPS
DOI: 10.5897/IJPS11.151
ISSN 1992 - 1950 ©2011 Academic Journals

Full Length Research Paper

Statistical optimization for process parameters to reduce variability of 32 nm PMOS transistor threshold voltage

H. A. Elgomati[1]*, B. Y. Majlis[1], I. Ahmad[2], F. Salehuddin[2], F. A. Hamid[2], A. Zaharim[3], T. Z. Mohamad[4] and P. R. Apte[5]

[1]Institute of Microengineering and Nanoelectronics, Universiti Kebangsaan Malaysia (UKM) 43600 Bangi, Selangor, Malaysia.
[2]College of Engineering, Universiti Tenaga Nasional (UNITEN) 43009 Kajang, Selangor, Malaysia.
[3]Faculty of Engineering and Built Environment, Universiti Kebangsaan Malaysia (UKM)[3] 43600 Bangi, Selangor, Malaysia.
[4]Test 2 Operation, Freescale (M) Sdn. Bhd. P. O. Box 1001, Jln Semangat 47300 Petaling Jaya, Selangor D.E., Malaysia.
[5]Indian Institute of Technology (IIT) Bombay, Powai, Mumbai-400076, India.

Accepted 01 April, 2011

This paper explains our investigation of the effect on 32 nm PMOS device threshold voltage (V_{TH}) by four process parameters, namely HALO implantation, Source/Drain (S/D) implantation dose, compensation implantations, and silicide annealing time. Taguchi method determines the setting of process parameters in experimental design while analysis of variance (ANOVA) determines the influence of the main process parameters on threshold voltage. The fabrication processes of the transistor were performed by ATHENA fabrication simulator, while the electrical characterization of the device was done by an ATLAS characterization simulator. These two simulators were combined and the results were analyzed by Taguchi's method in order to aid in design and optimizing process parameters. Threshold voltage (Vth) results were used as the evaluation parameters. The results show that the V_{TH} value of –0.10319 V is achieved for a 32 nm PMOS transistor. In conclusion, by utilizing Taguchi's method to analyze the effect of process parameters, we can adjust threshold voltage (V_{TH}) for PMOS to a stable value of –0.10319 V that is well within ITRS prediction for a 32 nm PMOS transistor.

Key words: 32 nm PMOS device, HALO, compensation implantation, S/D implantation, threshold voltage, Taguchi's method.

INTRODUCTION

Structural physical downscaling of Complimentary Metal-Oxide Semiconductor (CMOS) started in the early 1970s (Taur, 1995), and it has given us many challenges and technology discoveries. The speed of downscaling has been showing exponential growth since then, as end users crave for more new technologies in their daily life. One of the main complications in producing a smaller transistor is to control the threshold voltage (V_{TH}). Following Moore's law, the number of transistors per silicon area doubled every 18 months (Taur, 1995), and with wider use of mobile applications and miniaturized equipments, has further led to reducing the area available to put the transistors. Wafer fabrication process parameter variation increased and has been perceived as one of the major barriers to further downscaling the technology (Liang and Nikolic, 2006).

Threshold voltage mismatch is one of the main analogue performance indicators of CMOS technology, since it

*Corresponding author. E-mail: hus_7119@yahoo.com.

determines the accuracy-speed-power trade-off of the basic analogue building blocks. The lower level threshold voltage mismatch is largely due to doping fluctuations (Liang and Nikolic, 2006; Burenkov et al., 2000). As a result, it complicates our task to get the right threshold voltage (V_{TH}) value for the transistor and also to control the gate leakage current to an acceptable level. Reaching 32 nm, we are almost at the extreme lower limit of the silicon oxide thickness at the gate as an insulator. In this case, we studied the effect of four parameters that are widely being used in CMOS wafer fabrication processes before high-K dielectric material being introduced to see the possibility of still achieving a working PMOS transistor by sticking with SiO_2. The four fabrication factors selected and analyzed are HALO implantation dose, Source/Drain (S/D) implantation dose, compensation implantation dose and silicide annealing temperature.

For PMOS, halo implantation is done by implanting P-type impurities in a desired depth in the semiconductor substrate prior to forming P-channel lightly doped source/drain areas. Then, moderately to heavily doped source/drain regions are formed, followed by activation annealing. The halo implants followed to form halo structures at the desired location, thereby reducing short channel effects, such as subsurface punch-through. Compensation implantation is performed to minimize transistor side capacitance (Curello et al., 2002). This will be very important to reduce transistor delay time and to ensure that the transistor gives the expected accurate switching performance. Phosphorous is used as impurity for this purpose for both NMOS and PMOS (Han et al., 2005).

The third factor is SiO_2 thickness. Reduction of gate oxide thickness results in an increase in the electric field across the oxide. The higher electric field coupled with low oxide thickness results in tunnelling of electrons from inverted channel to gate (or vice versa) or from gate to source/drain overlap region (or vice versa). There are two types of different tunnelling happening, 1) direct tunnelling and 2) Fowler-Nordheim (FN) tunnelling. The gate leakage of a micro device comes mostly from direct tunnelling. In scaled devices (with oxide thickness < 3 nm), the tunnelling mechanism occurs through the trapezoidal energy barrier and is known as direct tunnelling (Weiqiang et al., 2009). The oxide thickness is varied in three levels to be used with other parameters in Taguchi analysis.

This can even result in the transistor being turned-ON even when $V_G < V_{TH}$. As such, it is critical to get the right SiO_2 thickness for a working PMOS transistor. The final factor is the annealing time for self-aligned metal silicide technology. This silicide has been widely used to reduce resistance of polysilicon gates. Metal silicides such as titanium silicide ($TiSi_2$), tungsten salicide (WSi_2), cobalt salicide ($CoSi_2$) and nickel salicide ($NiSi_2$) are widely used for this purpose. These metals react with polysilicon, to form metal silicide layer that possesses better physical and electrical properties to interface with aluminium. The silicide need to be optimally annealed in order to obtain a good ratio of metal silicide to silicon in the gate structure (Maszara, 2005).

Taguchi method is a technique for designing and performing experiments in order to investigate processes where the output depends on many factors (variable, inputs) without having tediously and uneconomically run of the process using all possible combinations of values. The technique could be systematically chosen in certain combinations of variables and yet possible to separate their individual effects. In Taguchi's methodology, the desired design is finalized by selecting the best performance under the given condition (Lochner and Matar, 1990; Nunes et al., 2002, 2004). The tool used in Taguchi's method is the orthogonal array (OA). OA is the matrix number arranged in column and row. The Taguchi employs a generic signal to noise ratio (S/N) to quantify the present variation. These S/N ratios are to be used as measures of the effect of noise factors on performance characteristics. S/N ratio takes into account both amount of variability in the response and data and closeness of the average response target. There are three S/N ratios available depending on the type of characteristics namely, smaller the best, nominal is best (NB) and larger is better.

Actual fabrication in semiconductor industry is extremely expensive and time consuming, with the complexities increased exponentially as we reach nanometer regime. The robust nature of Taguchi enables us to reduce project duration by varying the factors at three different levels and running only nine sets of experiment (per L_9 orthogonal array) as suggested by Taguchi (Roy, 2001; Sharma et al., 2005; Syrcos, 2003). By analyzing the result accordingly, we are able to predict the optimum fabrication recipe in producing a 32 nm PMOS with the V_{TH} value of –0.10319 V. The value is well within ITRS prediction for 32 nm transistor (ITRS, 2008).

MATERIALS AND METHODS

The substrate used for experiment was a silicon p type, <100> orientation (Wang et al., 2002; Burenkov et al., 2000). An oxidation layer, the top layer using dry oxygen, on a temperature of 970°C for 20 min. P-well implantation process was done, using this oxide layer as a mask. This was done using Boron as dopant with a dose of 3.75×10^{12} ions/cm^2 and the implantation energy of 100 keV. The wafer was tilted 7°. The silicon wafer then has undergone the annealing process. The process was at 910°C for 30 min in nitrogen and dry oxygen for 36 min in order to ensure that boron atoms being spread properly in the wafer. The masking oxide was then etched. The following step was to produce Shallow Trench Isolator (STI) of 130 Å thickness (Sleight et al., 2006). In order to form STI layer, the wafer was oxidised in dry oxygen for 25 min at 900°C. Then, a 1500 Å nitride layer was deposited on top of the oxide layer by applying low pressure chemical vapour deposition process (LPCVD), followed by a photo resist deposition with a thickness of 1.0 µm. Then, the photo resist and the nitride were etched using reactive ion etching

Table 1. Experimental layout using $L_9(3^4)$ orthogonal array.

Exp. no.	Process parameter level			
	A (Halo implant)	B (S/D implant)	C (Compensation implant)	D (Silicide anneal temp)
1	1	1	1	1
2	1	2	2	2
3	1	3	3	3
4	2	1	2	3
5	2	2	3	1
6	2	3	1	2
7	3	1	3	2
8	3	2	1	3
9	3	3	2	1

process (RIE) at the top of STI area. The trench depth of 3240 Å was achieved in 30 s process.

Thereafter, a sacrificial oxide layer was grown and then etched followed by a sacrificial nitride layer. The trench was then completed. To introduce a process noise (N1), in a second run of the device fabrication process, the diffusion temperature was increased to 901°C. The next process was to grow the gate oxide. In order to do this, the silicon wafer was oxidised with dry oxygen, at 825°C, at 1.0 a.t.m. for a short time. The short time is needed to ensure a very thin layer and not more than 1.1 nm of oxide thickness was grown. Then, the next step was to implant phosphorus and boron difluoride (BF_2) at both, N and P well active areas respectively, in order to adjust the threshold voltage, V_{TH} value. The dosages for phosphorus and boron were 1.75×10^{11} ions/cm^2 and 5.0×10^{11} ions/cm^2 respectively. The energy for both implantations was 5 keV and it was tilted at 7°. Polysilicon will then be deposited on the top of the wafer by thickness of 7.72 nm and then etched accordingly to produce the gate contact point as desired. Halo implantation then took place on both sides, P and N well active area, Indium with the dose was 2.40×10^{13} ions/cm^2, with the energy of 120 keV. It was tilted 30° while implanting for both P- and N-wells. The dosage was varied in order to get the optimum value as shown in Table 1. Nitride layer will then be deposited on top of the polysilicon gate and immediately etched to expose the top surface of the silicon layer. Then spacers were formed at each of the polysilicon sides, namely source and drain regions respectively. A silicon nitride layer of 0.0423 µm was deposited (ITRS, 2008).

Then it was etched away for the same thickness. Due to the nature of the substrate surface with gate, side wall spacers were created as the thickness at the gate sides, that was 0.0867 µm. Side wall spacers used as a mask for source and drain implantation (Jaeger, 2002). Then, there were source-drain implantations, prior to implantation of source and drain (Salehuddin et al., 2011), photo resist deposited and etched for source and drain area, firstly boron with dose of 1.0×10^{14} ions/cm^2, 12 keV implantation energy and was tilted at 7°, followed by phosphorous with dose of 6.55×10^{11} ions/cm^2, 12 keV implantation energy and was also tilted 7°. The next process was to diffuse the dopants at 900°C for 10 min. Thereafter, depositing an oxide mask on top of polysilicon gate was done in order to form a silicide structure. Cobalt silicide layer of 0.0867 µm was then deposited on top of the substrate and then was annealed by rapid thermal annealing process in a nitrogen environment. It was done at 900°C. However, the temperature was varied as in Table 1, in order to obtain three different thicknesses and ion distribution for optimisation.

Afterwards, the unwanted area of cobalt was etched away. The introduction of the second noise happened at the next step, where the annealing of the structure for 6 s, on a temperature of 910°C, nitrogen environment at 1 a.t.m. The noise (N2) was introduced by reducing the anneal temperature to 908°C. This annealing process was to deepen and spread the cobalt atoms into the polysilicon. The next process was the development of 0.3 µm Borophosphosilicate Glass (BPSG) layer (Sarcona et al., 1999). This layer act as pre metal dielectric (PMD). PMD contains silicon dioxide doped with boron and phosphorus. After Borophosphosilicate Glass (BPSG) deposition, the wafer underwent 20 min annealing at a temperature of 850°C (Sleight et al., 2006). The next process was compensation implantations using phosphorous, with a dose of 3.0×10^{13} ions/cm^2, 60 keV implantation energy respectively. The wafers were tilted (Hashim, 2009). Then followed by aluminium contact deposition. The wafer was then annealed for 20 s at 850°C. Then, aluminium layer was deposited on top of the structure and then etched accordingly, to form the metal contact for source and drain. At this juncture the transistor was completed. Then, the transistor underwent electrical characteristic measurement in order to find the leakage current.

Taguchi's method using L9 orthogonal array

In this work, an $L_9(3^4)$ orthogonal array which has 9 experiments was used. Four process parameters namely, source drain implantation, Compensation Source Drain implantation, Halo Implantation and Silicide annealing time. The values of the four process parameters at the different levels are listed in Table 1.The experimental layout for the process parameters using the $L_9(3^4)$ orthogonal array is shown in Table 2. The two noise factors will create four measurements for each row of experiment in the L9 array, thus leading to a set of experiments consisting of 36 runs. A set of four measurements for each row of L9 orthogonal array is the minimum number of results needed for our project using Taguchi analysis.

The 36 experiments are then run and the resulting VTH is recorded accordingly and analyzed. Taguchi's method calculates the effect of the factors to the result means and also to the SNR. From this, we can predict the factor that is most dominant to the result means and also the factor that is most dominant to the results SNR. Knowing each of those, we will determine the factors to be fixed and the one to be varied in the subsequent experiments to find the solution. The optimized results from Taguchi's method were then simulated, in order to verify the predicted optimal design. Details of the analysis are as follows.

Table 2. Process parameters and their levels.

Device	Symbol	Process parameter	Unit	Level 1	Level 2	Level 3
PMOS	A	Halo Implant	atom/cm^3	2.38 × 10^{13}	2.40 × 10^{13}	2.42 × 10^{13}
	B	S/D Implant	atom/cm^3	6.50 × 10^{11}	6.55 × 10^{11}	6.60 × 10^{11}
	C	Compensation Implant	atom/cm^3	2.9 × 10^{13}	3.0 × 10^{13}	3.1 × 10^{13}
	D	Silicide Anneal Temp	℃	890	900	910

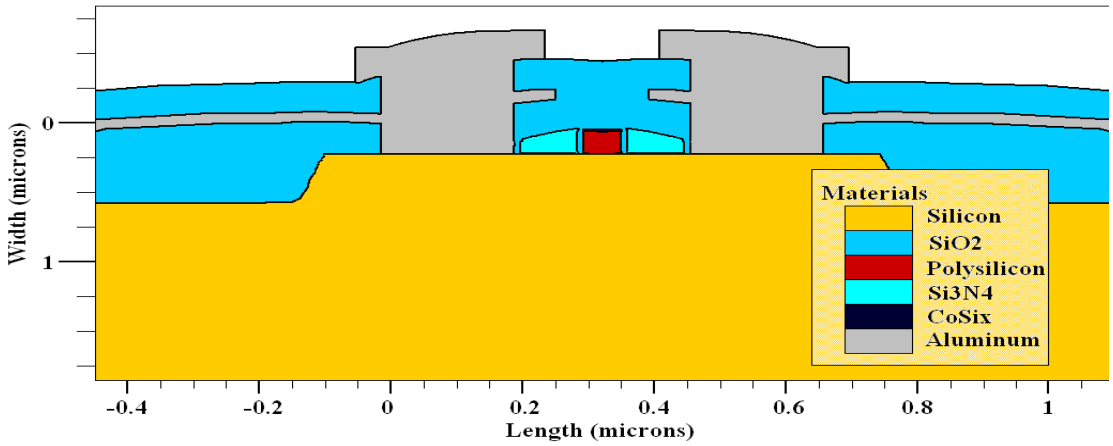

Figure 1. Completed PMOS transistor.

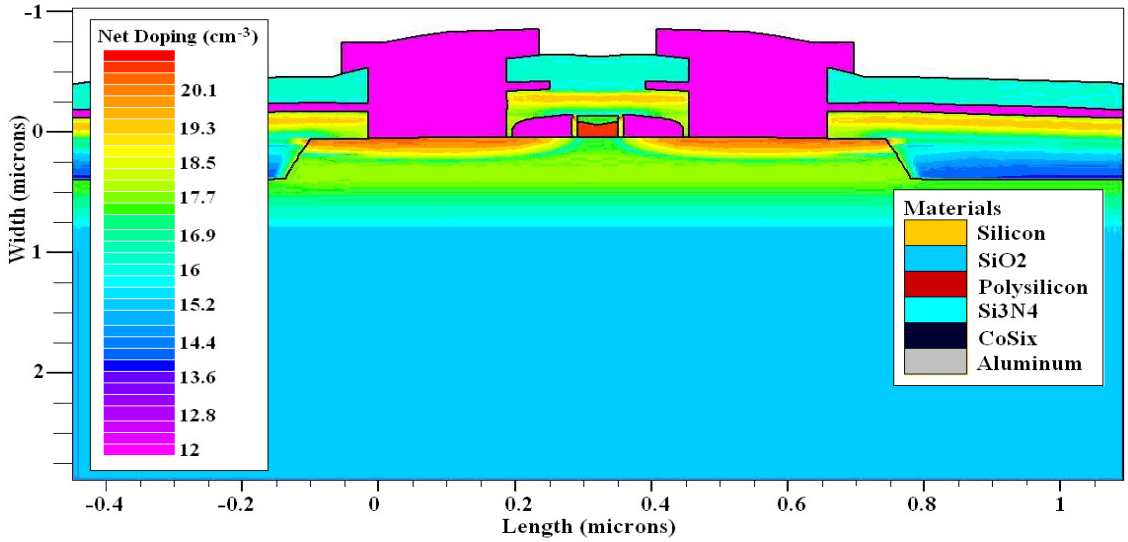

Figure 2. The doping profile of the PMOS transistor.

RESULTS AND DISCUSSION

Analysis of 32 nm PMOS transistors

Figure 1 shows the completed PMOS transistors while Figure 2 showing the doping profiles of the PMOS. The resulting values of V_{TH} were recorded and analyzed with Taguchi's method to get the optimal design. The experimental results, V_{TH}, for PMOS devices are shown in Table 3. Transistor V_{TH} should be classified under

Table 3. V_{TH} Values for PMOS device.

Exp. no.	Threshold voltage (volts)			
	$V_{TH}1$	$V_{TH}2$	$V_{TH}3$	$V_{TH}4$
1	-0.09377	-0.10846	-0.09146	-0.08979
2	-0.11463	-0.13717	-0.11761	-0.11455
3	-0.14249	-0.12857	-0.14473	-0.15062
4	-0.11937	-0.11971	-0.10469	-0.09832
5	-0.12494	-0.1196	-0.13088	-0.09868
6	-0.10471	-0.10297	-0.09276	-0.09669
7	-0.11489	-0.11756	-0.10197	-0.12222
8	-0.09821	-0.09315	-0.09153	-0.10406
9	-0.10544	-0.11729	-0.10357	-0.11736

Table 4. Mean, variance and S/N ratios for PMOS device.

Exp. no.	Mean	Variance	S/N ratio (mean)	S/N ratio (Nominal-the-Best)
1	-9.59E-02	7.31E-05	-2.04E+01	2.10E+01
2	-1.21E-01	1.18E-04	-1.83E+01	2.09E+01
3	-1.42E-01	8.72E-05	-1.70E+01	2.36E+01
4	-1.11E-01	1.15E-04	-1.91E+01	2.03E+01
5	-1.19E-01	1.96E-04	-1.85E+01	1.85E+01
6	-9.93E-02	3.08E-05	-2.01E+01	2.51E+01
7	-1.14E-01	7.52E-05	-1.88E+01	2.24E+01
8	-9.64E-02	3.78E-05	-2.03E+01	2.39E+01
9	-1.11E-01	5.54E-05	-1.91E+01	2.35E+01

Table 5. Mean response for the threshold voltage.

Device	Symbol	Process parameter	Mean response			Total mean S/N	Max - Min
			Level 1	Level 2	Level 3		
PMOS	A	Halo Implant	-18.56	-19.24	-19.42	-19.08	0.86
	B	S/D Implant	-19.45	-19.06	-18.71		0.74
	C	Compensation Implant	-20.25	-18.86	-18.12		2.13
	D	Silicide Anneal Temp	-19.33	-19.09	-18.81		0.52

nominal-the-best quality characteristics. The result means is desired to be closest or equal to a given target value, which is known as nominal value (Naidu, 2008). The S/N Ratio, η can be expressed as (Douglas, 2005):

$$\eta = 10\mathrm{Log}_{10}\left[\frac{\mu^2}{\sigma^2}\right] \quad (1)$$

While μ is mean and σ is variance. By applying Equations (1), the η for each device was calculated and given in Table 4.

The effect of each process parameter on the mean and S/N ratio at different levels can be separated out because the experimental design is orthogonal. The mean and S/N ratio (nominal the best) for each level of the process parameters are summarized in Tables 5 and 6. The total mean for each one are calculated and from this maximum to minimum effect of each factor can be calculated. Figure 3 shows the S/N ratio graphs of PMOS devices, where the dashed line is the value of the total mean of the S/N ratio. Basically, the larger the S/N ratio, the quality characteristic for the threshold voltage is better. The closer the quality characteristic value to the target, the better the product

Table 6. S/N Ratio for the threshold voltage.

Device	Symbol	Process parameter	S/N ratio (Nominal-the-Best)			Total mean S/N	Max - Min
			Level 1	Level 2	Level 3		
PMOS	A	Halo Implant	21.84	21.29	23.25	22.13	1.41
	B	S/D Implant	21.21	21.12	24.05		2.93
	C	Compensation Implant	23.32	21.55	21.52		1.80
	D	Silicide Anneal Temp	21.00	22.79	22.59		1.79

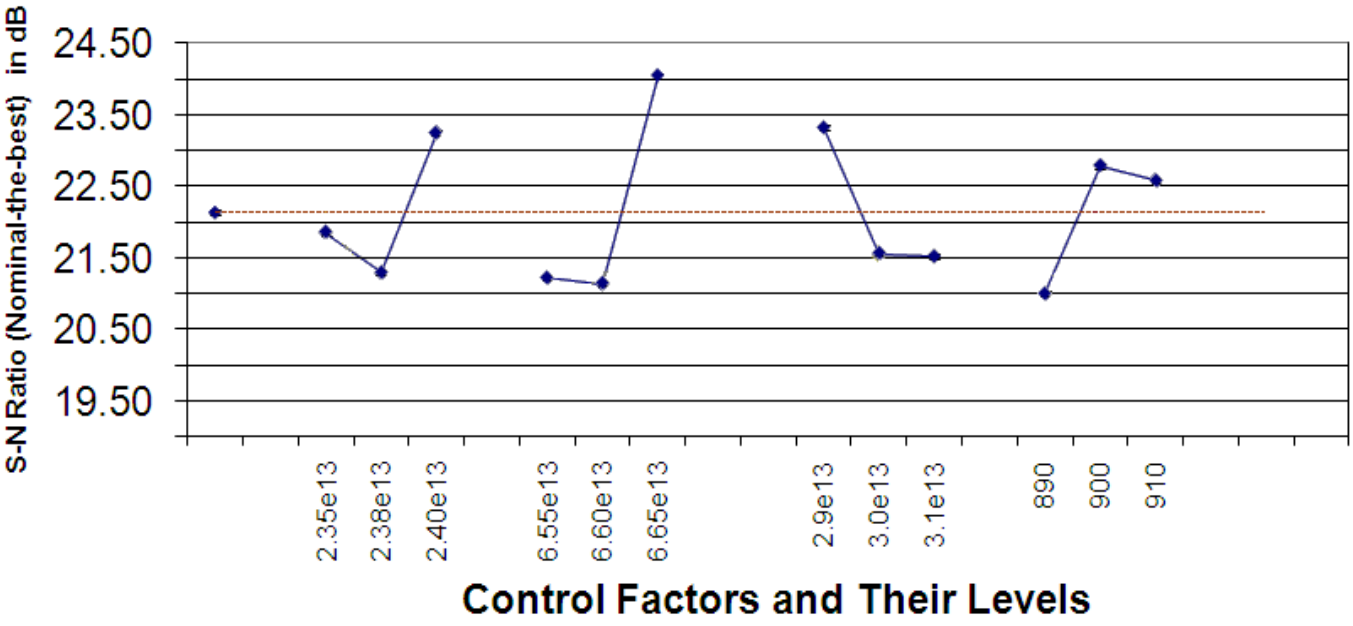

Figure 3. S/N graph for threshold voltage in PMOS device.

Table 7. Result of ANOVA for PMOS device.

Symbol	Process parameter	Degree of freedom	Sum of square	Mean square	Factor effect on S/N ratio (%)	Factor effect on mean (%)
A	Halo Implantation	2	6	3	18	13
B	S/D Implantation	2	17	8	48	9
C	Compensation Implantation	2	6	3	18	74
D	Silicide Anneal Temperature	2	6	3	16	4

quality will be (Naidu, 2008).

Analysis of variance (ANOVA)

The priorities of the process parameters with respect to the V_{TH} are investigated to determine more accurately the optimum combinations of process parameters. The result of ANOVA for the PMOS device is presented in Table 7. The factor effect percentage on S/N ratio indicates the priority of a factor (process parameter) in reducing variation. A factor with a higher percent contribution will

Table 8. The optimized factors for PMOS device.

Symbol	Process parameter	Unit	Best value
A	Halo Implantation	atom/cm^3	2.35E13
B	S/D Implantation	atom/cm^3	6.65E11
C	Compensation Implantation	atom/cm^3	3.10E13
D	Silicide Anneal Temperature	℃	910

Table 9. Results of the confirmation experiment.

Device	Symbol	Process parameter	Unit	Best value
PMOS	A	Halo implantation	atom/cm^3	2.35E13
	B	S/D implantation	atom/cm^3	6.65E13
	C	Compensation implantation (as an adjustment factor)	atom/cm^3	3.10E13
	D	Silicide anneal temperature	℃	910

Table 10. Results of further runs of confirmation experiment with added Noise (Rs).

Device	V_{TH} (n1,n1)	V_{TH} (n1,n2)	V_{TH} (n2,n1)	V_{TH} (n2,n2)
PMOS	-0.10297	-0.10344	-0.10295	-0.10339

have a greater influence on the resulting device performance. The result of ANOVA for the PMOS device is presented in Table 7. The results clearly show that the S/D implantation (48%) has the most dominant impact to the resulting threshold voltage in PMOS device, whereas compensation implantation was the second ranking factor (18%). The percent effect on S/N ratio of halo implantation and silicide anneal temperature are much lower being 18 and 16% respectively. The optimized factors for PMOS device which had been suggested by Taguchi's method are shown in Table 8.

For the PMOS device, compensation implantation was defined as an adjustment factor because of its minimal effect on SNR (18%) but large effect on means (74%). Several simulations have been done with different values of compensation implantation to get the threshold voltage at nominal value or target value. The compensation implantation was adjusted within 2.90×10^{13} to 3.10×10^{13} until the value of threshold voltage closer to -0.103 V. By doing the value sweep, the compensation implantation doping as the optimum solution for fabricating a 32 nm PMOS transistor was found at 2.97×10^{13} atoms/cm^3. From the aforementioned parameters as shown in Table 9, another simulation was performed to verify the accuracy of the Taguchi method of prediction. The results show that the threshold voltage for 32 nm PMOS transistor is -0.10297 V. Adding noise factors to this simulation and having run them we got the results as shown in Table 10. From Table 10, for PMOS, the mean is -0.10319 V with S/N ratio of 34. The values are well within the target set by ITRS and Figure 4 shows the relationships of the I_D-V_D for 32 nm PMOS transistors.

Conclusion

For PMOS, we found that compensation implantation has the largest effect to the value of resulting transistor V_{TH}. The experiment shows for PMOS, the effect of each factor are at different levels and are not as predicted to be almost the same. This experiment also proves that Taguchi Analysis can be effectively used in finding the optimum solution in producing 32 nm PMOS transistor. At this technology juncture, we still manage to find a working transistor with threshold voltage and leakage current well within International Technology Roadmap for Semiconductor (ITRS) prediction. In this research, compensation implantation has the strongest effect on the response characteristics in PMOS devices.

ACKNOWLEDGMENT

The authors would like to thank the Ministry of High Education (MOHE) for their financial support, of the Photonic Lab Universiti Kebangsaan Malaysia (UKM) and the Institute of Micro-engineering and Nanoelectronic, and also use this chance to thank Universiti Tenaga Nasional (UNITEN) for the moral support throughout the project.

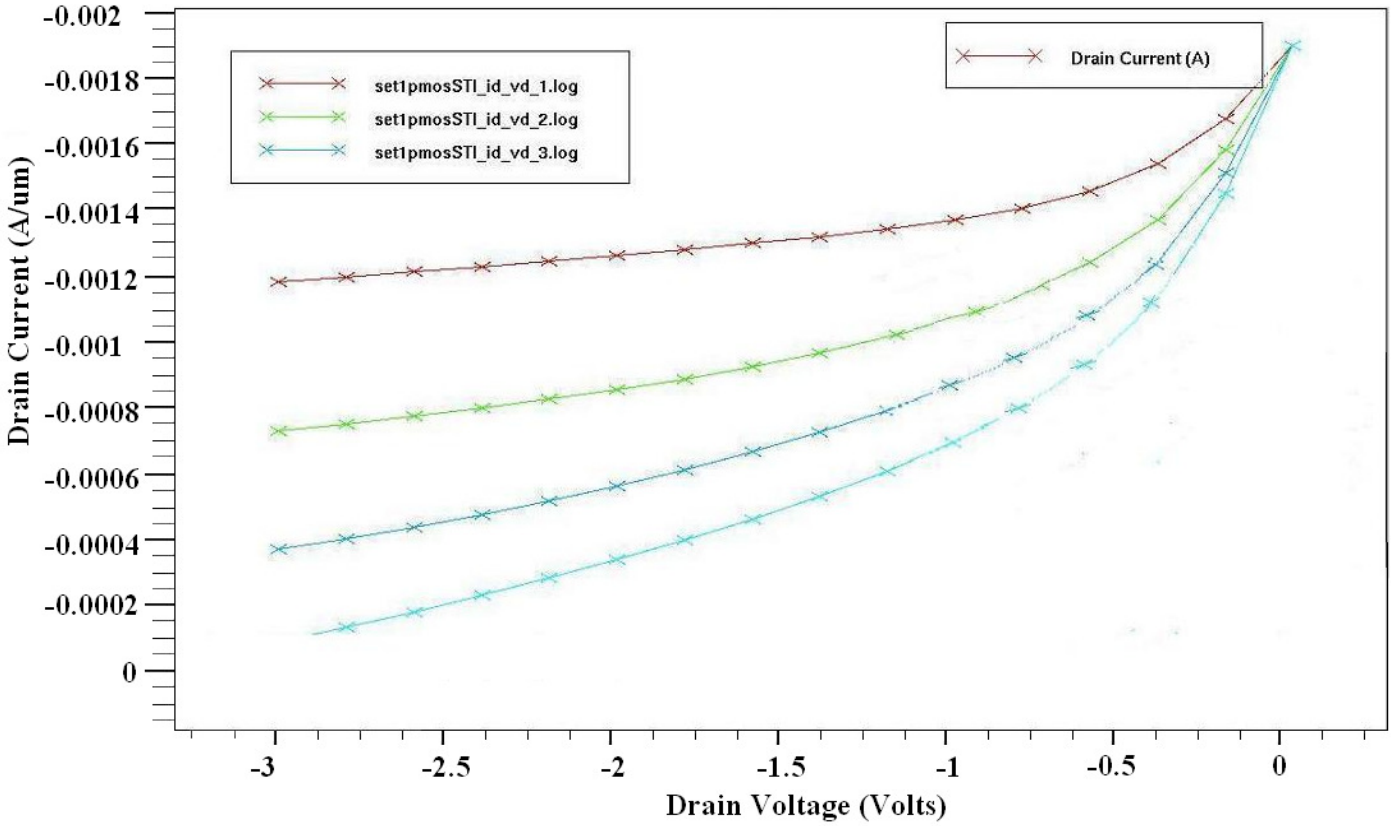

Figure 4. I_D-V_D relationships for 32 nm PMOS transistor.

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