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Full Length Research Paper

Effect of gate electrode work function in conventional and junctionless FinFETs

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This paper investigates the effect of gate electrode work function in 30 nm gate length conventional and junctionless FinFETs using technology computer-aided design (TCAD) simulations. DC parameters, threshold voltage (v_t), drive current (I_{on}) and output resistance (R_o), and RF parameters, unity gain cut-off frequency (f_t), non-quasi static (NQS) delay and input impedance (Z_{11}) are investigated. Junctionless devices being bulk conductive behaves differently with respect to work function variation compared to surface conducting conventional devices. The rate of change in V_t and I_{on} with respect to work function, in junctionless devices, is slower compared to conventional devices. Owing to better drain induced barrier lowering (DIBL) performance, junctionless devices have higher output resistance. In conventional devices, f_t is not sensitive for most of the work function range due to the screening effect of the inversion layer whereas junctionless device shows strong dependency on the work function.

Key words: FinFET, Junctionless transistor, work function, drain induced barrier lowering (DIBL), technology computer-aided design (TCAD).

INTRODUCTION

Down-scaling in the conventional bulk complementary metal oxide semiconductor (CMOS) technology is facing critical issues such as short-channel effects and high power dissipation in MOSFET devices. Multi-gate devices are thought as a potential alternative to MOSFETs. Among the multi-gate devices, junctionless devices (Colinge et al., 2010a, b; Lee et al., 2010a) have gained significant attention as potential candidates for replacing the traditional CMOS technology in the nanometer regime.

Multi-gate devices heavily rely on gate electrode work function engineering. The effect of work function in 16 nm gate length conventional FinFETs has been explored by Hwang et al. (2009, 2010). The impact of work function on RF characteristics like unity gain cut-off frequency (f_t) and gate capacitance have been discussed in the above said references.

Junctionless devices being bulk conductive, the effect of gate electrode work function engineering will be different from that of conventional FinFETs. Variation in DC characteristics like threshold voltage, subthreshold slope (SS), drain induced barrier lowering (DIBL) and drive current with respect to gate length (both physical and effective), fin width, doping concentration, temperature and line edge roughness (LER) have been reported for junctionless and inversion mode devices (Lee et al., 2010b, c; Colinge et al., 2009; Choi et al., 2011; Souza et al., 2011; Leng et al., 2011). But a comprehensive understanding of the impact on the work function of the junctionless device is yet to be explored.

SIMULATOR AND SIMULATION METHODOLOGY

TCAD simulator

Sentaurus TCAD simulator from Synopsys (2008-2009) is used for this study. All the simulations are carried out at 2D level. The simulator has many facilities and the following modules are used in this study:

i. Sentaurus structure editor (SDE): This is used to create the device structure, to define doping, to define contacts, and to generate mesh for device simulation,
ii. Sentaurus device simulator (SDEVICE): This is used to

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simulate all DC, AC and transient characteristics. In the simulations, doping dependency of mobility, effect of high and normal electric fields on mobility, velocity saturation and carrier quantization are used,
iii. Tecplot and Inspect: These are used to view the results.

Simulation methodology

The device structures are generated using SDE. Figure 1(a) shows conventional double gate (DG) transistor. Figure 1(b) depicts the junctionless double gate (DG) transistor. The current values of the two devices are calibrated against the published experimental results by tuning the Silicon parameter library file (Kranti et al., 2007; Lee et al., 2010b; Leung and Chui, 2011). After calibration, the device dimensions are brought to the requirements as given in Table 1. Figure 2 shows the simulated I_d-V_g characteristics for double gate (DG) with I_{off} matched = 0.59 nA/µm.

From the saturation I_d-V_g characteristics, V_t and I_{on} are extracted and from I_d-V_d characteristics, R_o is extracted for different gate bias. From the standard AC simulations f_t is extracted when $|Y_{21}/Y_{11}|$ equals one, and it strongly depends on the gate bias. At various gate biases f_t is calculated and the maximum of them is taken as f_t. Non-quasi static (NQS) delay is extracted using transient simulation, that is, a small time varying AC signal along with a DC bias (0.5V) is applied to the gate. The delay between the applied gate signal and the drain current is measured to get the NQS delay. The real part and imaginary part of the input impedance (Z_{11}) are calculated from the standard AC simulations. TCAD simulation yields Y-parameter matrix which are converted into Z-parameter using standard formulae.

RESULTS AND DISCUSSION

The work function (WF) is varied from 4.4 to 5 eV and 5.3 to 5.9 eV for conventional and junctionless devices, respectively. Studies related to gate electrode work function engineering can be found in (Kang et al., 2006; Luan et al., 2006). Outside these ranges, threshold voltage either becomes too high resulting in very less I_{on} or too low resulting in too high I_{off}. As already stated, DC parameters, V_t, I_{on} and R_o and RF parameters f_t, NQS delay and Z_{11} are extracted with respect to this work function variation.

Effect of work function on V_t, I_{on} and R_o

Figure 3 depicts the variation of V_t w.r.t WF for both the conventional and junctionless devices. This V_t extraction is done by means of peak g_m method. It can be seen from Figure 3 that V_t increases for both conventional and junctionless device. Another observation from Figure 3 is that the work functions in the range of 4.6 to 5 eV for conventional FinFETs, and 5.3 to 5.8 eV for junctionless FETs offers similar V_t. Figure 4 and 5 show the variation of conduction band energy along the channel for various WF, for conventional and junctionless DG respectively, with drain @ 1 V and gate @ 0 V. Since the increase in WF provides more barrier V_t increases with WF.

The effect of gate-channel work function difference on channel charge carriers is less in bulk conducting junctionless devices compared to surface conducting conventional devices which means that the rate of increase in V_t w.r.t work function change should be smaller in junctionless devices compared to conventional devices. This behavior is clearly seen in Figure 3.

Figure 6 shows the variation of I_{on} w. r. t work function, for conventional and junctionless devices with V_{GS} = 1V. It can be seen from Figure 6 that work functions in the range of 4.7 to 5 eV for conventional FinFETs, and 5.3 to 5.7 eV for junctionless FETs give similar I_{on}. Similar to V_t behavior, the rate of change in I_{on} w.r.t work function change is smaller in junctionless devices compared to conventional FinFETs. This can be again reasoned out in a similar manner as that of V_t variation w.r.t work function. Figure 7 shows the output resistance versus work function plots of conventional and junctionless devices, for different gate biases. As expected, due to less drain induced barrier lowering (DIBL), junctionless devices offer higher output resistance, for the given bias.

Effect of work function on f_t, NQS delay and Z_{11}

Figure 8 depicts the f_t variation w.r.t work function. It can be observed from Figure 8 that f_t in conventional devices is almost independent of work function variation. But, the junctionless devices show variation in f_t when work function is changed. Gate capacitance (C_{gg}) in conventional devices is less sensitive to work function because of the screening effect which is normally observed in the inversion mode devices (Hwang et al., 2010). f_t also did not show any significant change w.r.t work function. But, C_{gg} in junctionless devices show significant dependency on work function. C_{gg} combined with the trans-conductance (g_m) at bias points where f_t is extracted, results in the f_t behavior w. r. t work function as shown in Figure 8.

Figure 9 shows the NQS delay versus work function of conventional and junctionless devices, for 200 GHz. For both the devices, the NQS delay increases as expected. Once again, the rate of increase is less in junctionless devices compared to that of the conventional device because delay normally follows the trend of V_t. Figures 10 and 11 depict the real (ReZ_{11}) and imaginary (ImZ_{11}) part of Z_{11} versus work function, for the conventional and junctionless devices for two different frequencies of 1 and 10 GHz. To reason out the results of Figures 10 and 11, the following expression for the input impedance could be used (Ponton et al., 2009).

$$Z_{11} = \frac{1}{g_m} \cdot \frac{1}{1 + j\frac{f}{\frac{f_t}{2}}} \quad (1)$$

The above expression can be used only for reasoning out the trends of Figures 10 and 11. They need not predict

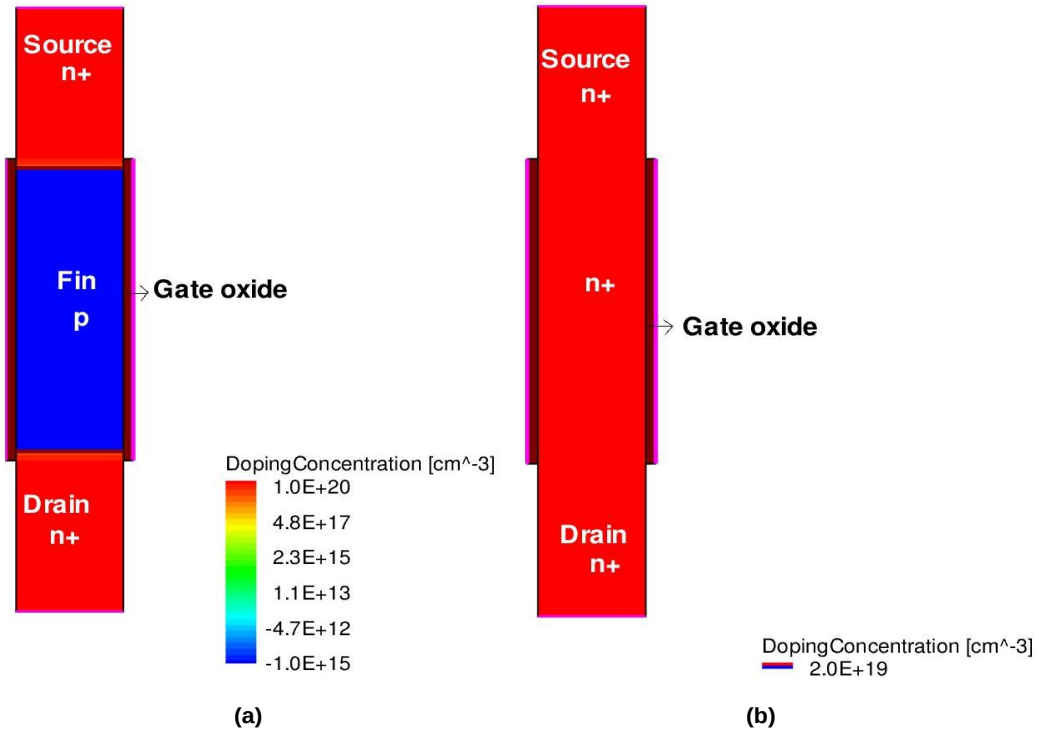

Figure 1. (a) 2-D structure of conventional DG (b) 2-D structure of junctionless DG.

Table 1. Dimensions and process parameters of the Conventional DG and Junctionless DG.

Process parameters	Conventional DG	Junctionless DG
Gate length (L_g)	30 nm	
Fin width (W)	10 nm	
Gate oxide thickness (T_{ox})	1 nm	
Channel doping (N_{ch})	1e15/cm^3	2e19/cm^3
Source/drain doping (N_{sd})	1e20/cm^3	2e19/cm^3
Supply voltage (V_{dd})	1 V	

the correct values of input impedance. The combined behavior of g_m, and f_t (which is again a function of g_m, and also C_{gg}) give rise to the trends seen in Figures 10 and 11. It has been reported that g_m for junctionless devices is lower compared to conventional devices (Doria et al., 2011). So, it is expected that the junctionless devices will show larger ReZ_{11} and ImZ_{11} compared to conventional devices.

Conclusion

The effects of gate electrode work function on DC parameters, V_t, I_{on}, R_o and RF parameters, f_t, NQS delay and Z_{11} were studied in 30 nm gate length conventional and junctionless FinFETs using TCAD simulations. Conventional devices are sensitive to DC parameters and not very sensitive to RF parameters when gate electrode work function is varied. Junctionless devices are sensitive to both DC and RF parameters for work function variation. Due to its bulk conduction property, variation of V_t and I_{on} with respect to work function is smaller. Due to the screening effect of the inversion layer, f_t in conventional devices was insensitive to work function variation whereas junctionless devices show dependency on work function. NQS delay w.r.t work function follows V_t trend for both devices.

ACKNOWLEDGEMENT

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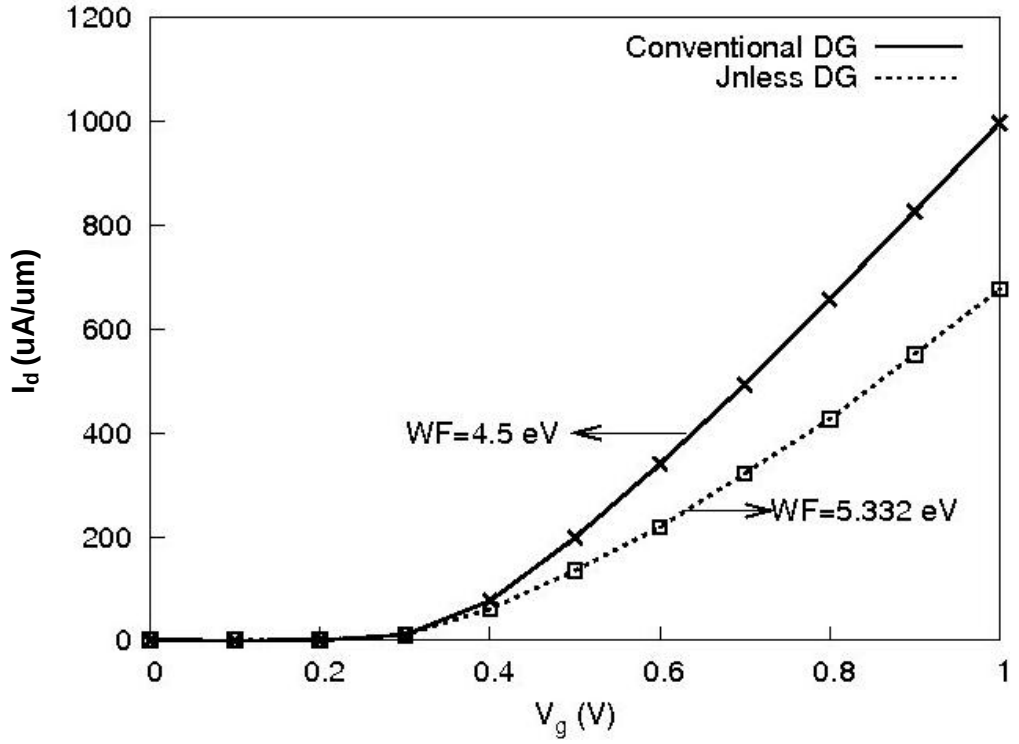

Figure 2. Simulated I_d-V_g characteristics of DG devices of gate length 30 nm with I_{off} = 0.59 nA/µm.

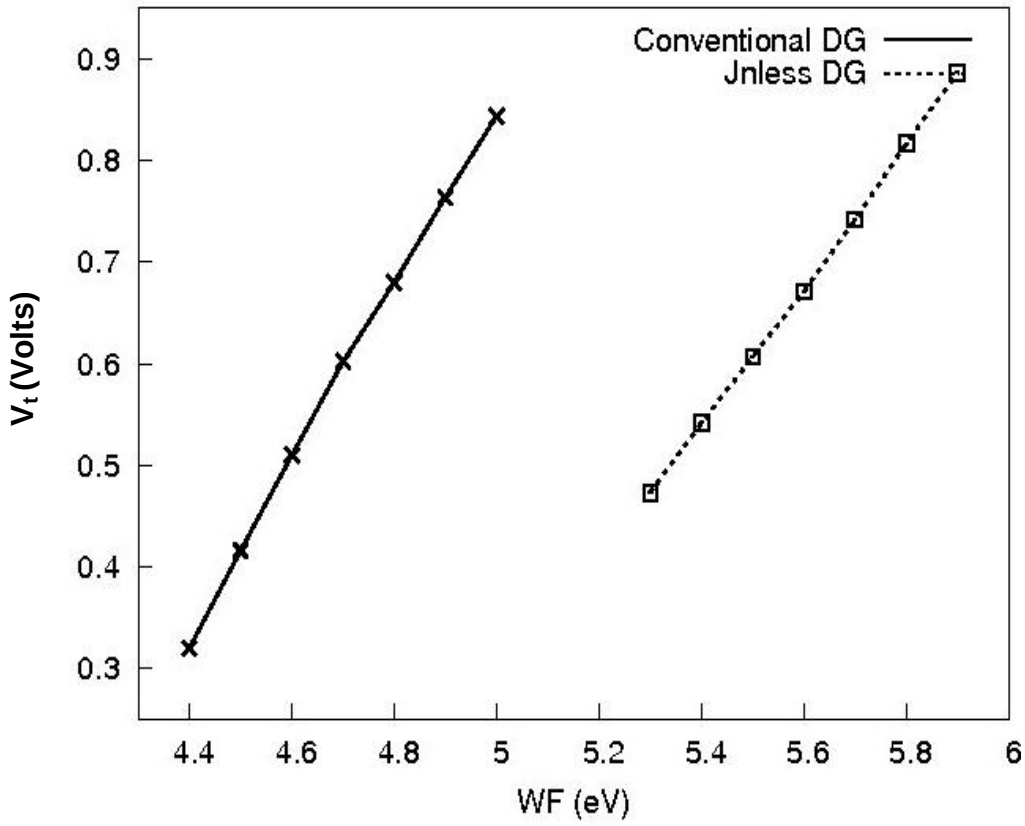

Figure 3. Variation of V_t w.r.t. WF for conventional and junctionless DG.

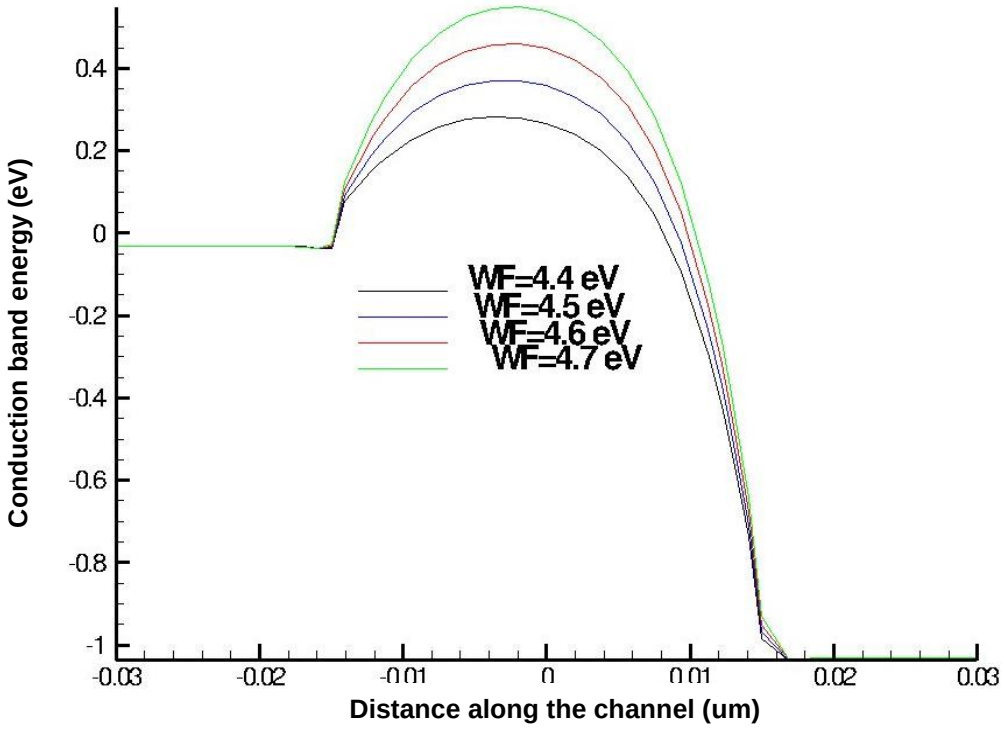

Figure 4. Band diagram of conventional DG along the channel w.r.t WF.

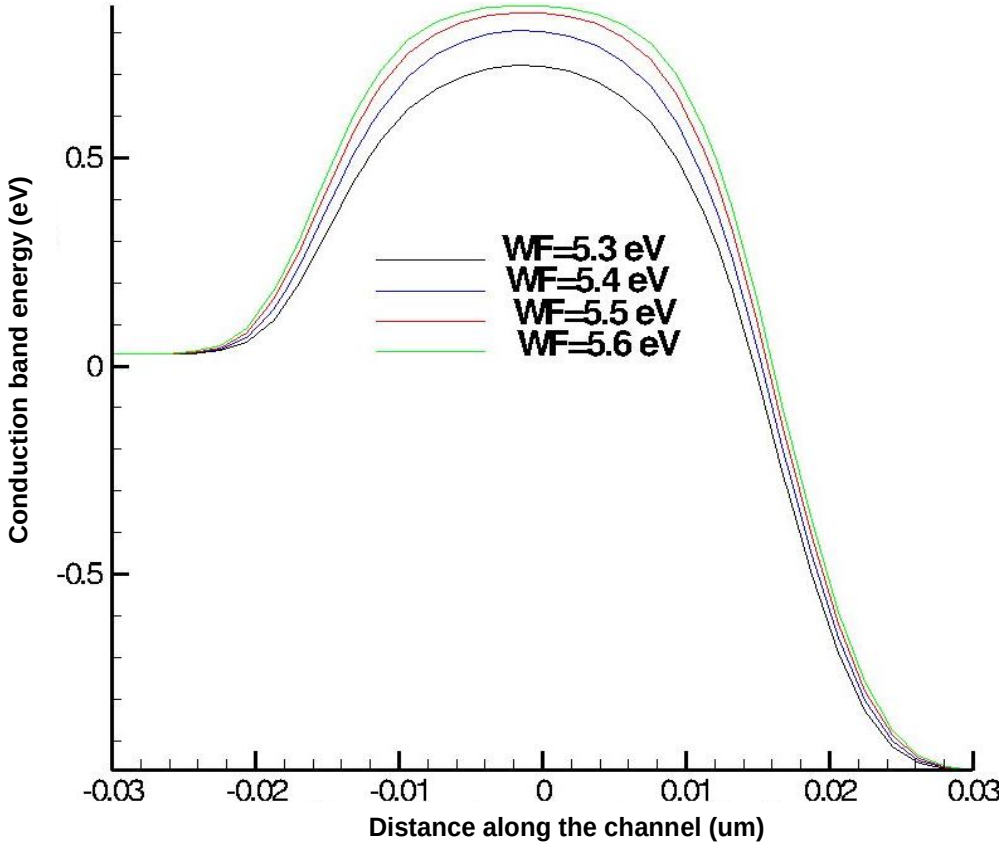

Figure 5. Band diagram of junctionless DG along the channel w.r.t WF.

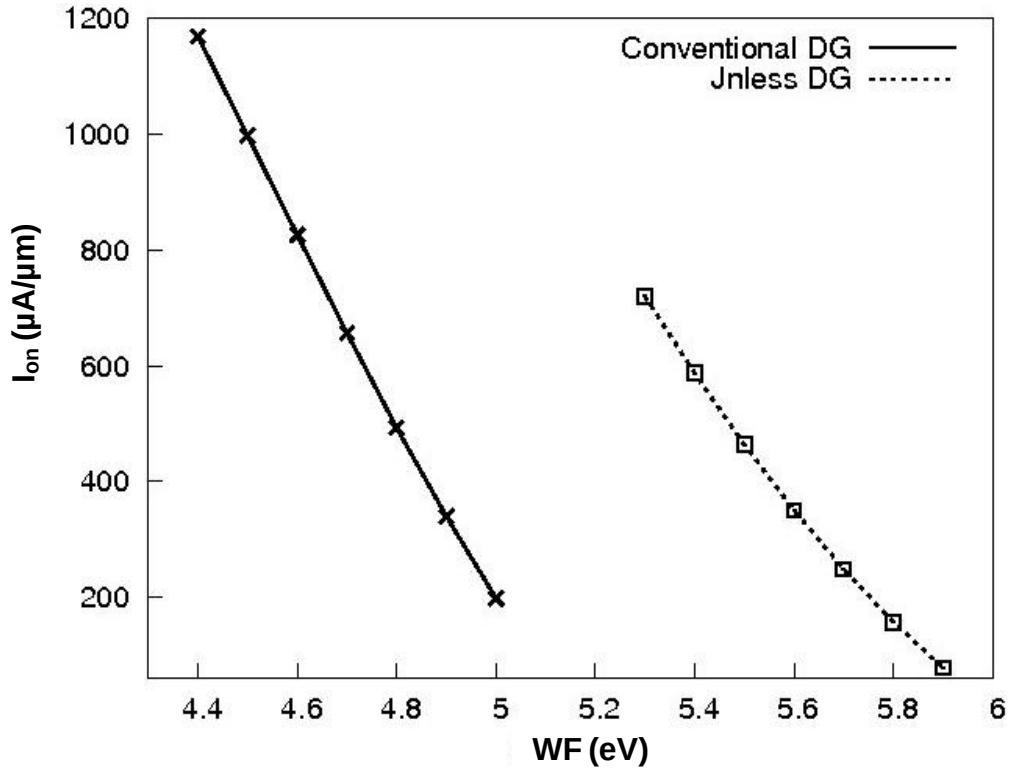

Figure 6. Variation of I_{on} w.r.t. WF for conventional and junctionless DG with V_{GS}=1 V.

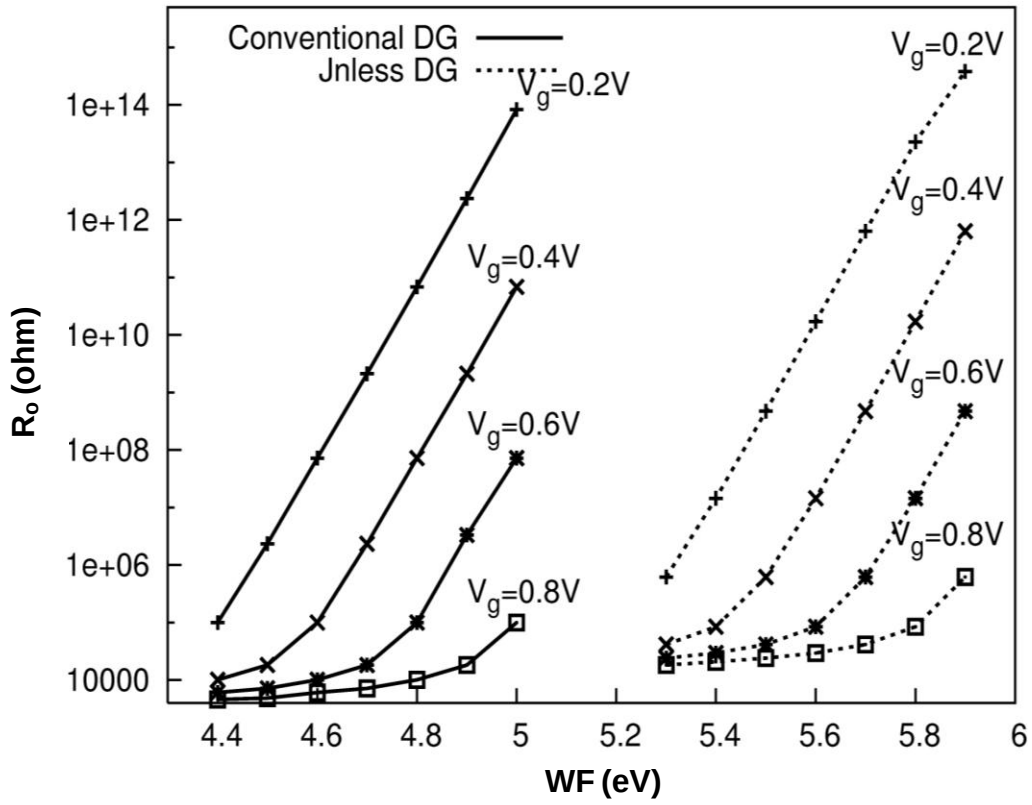

Figure 7. Variation of R_o w.r.t. WF for conventional and junctionless DG.

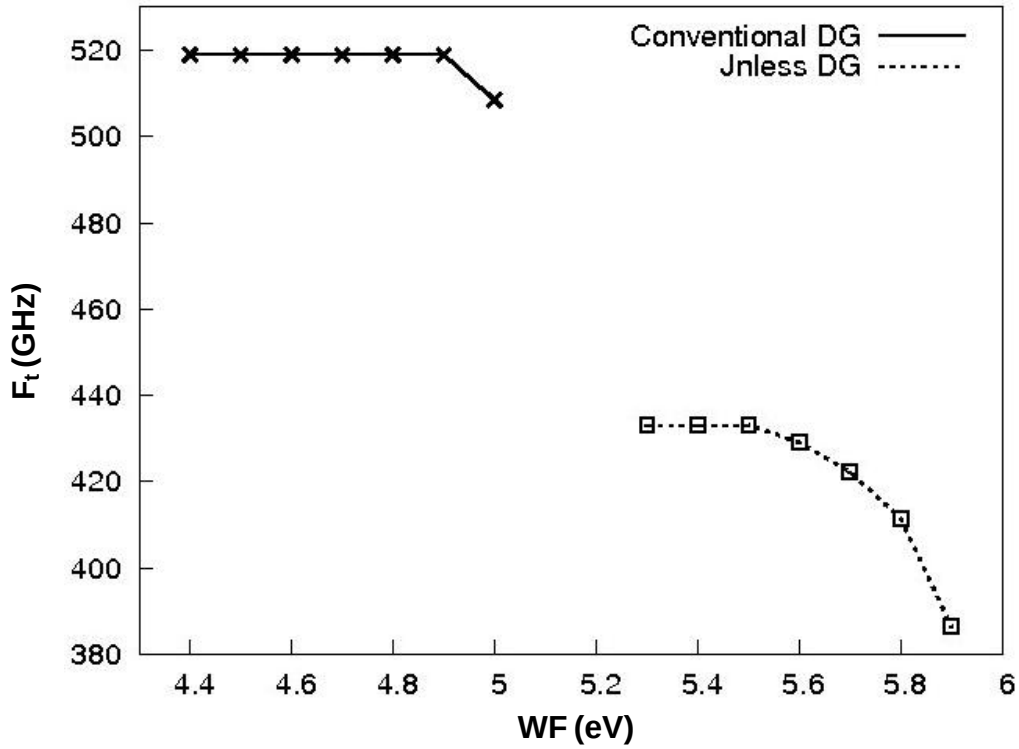

Figure 8. Variation of f_t w.r.t. WF for conventional and junctionless DG.

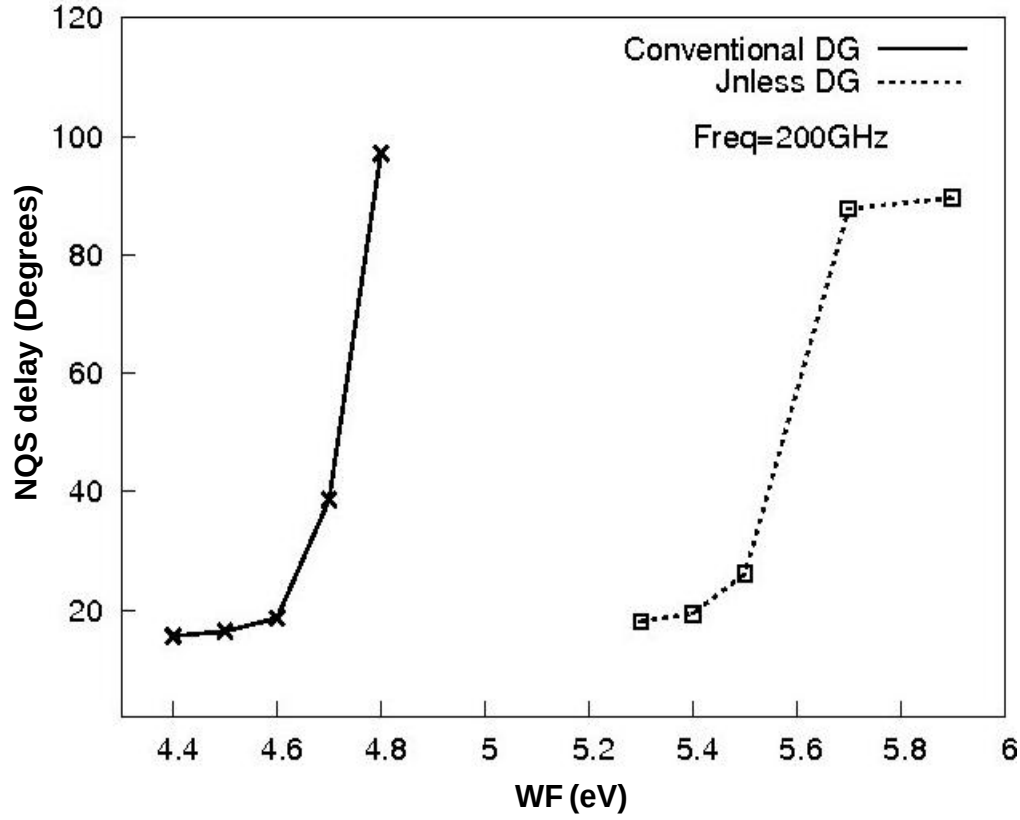

Figure 9. Variation of NQS delay w.r.t. WF for conventional and junctionless DG.

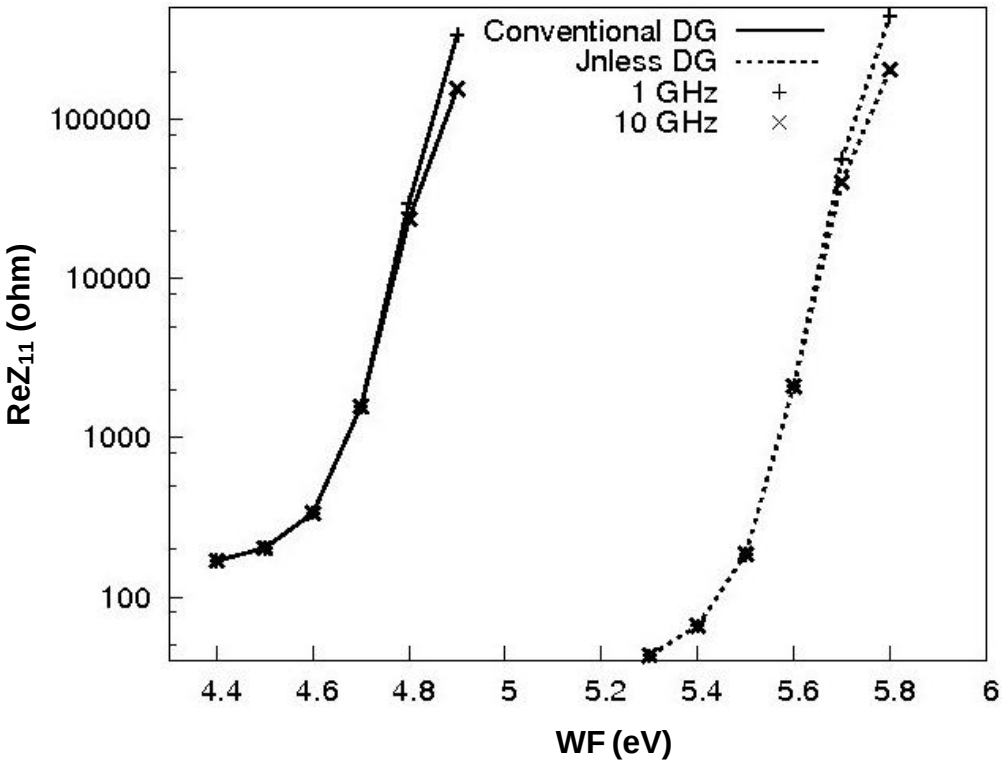

Figure 10. Variation of real part of Z_{11} w.r.t WF for conventional and junctionless DG.

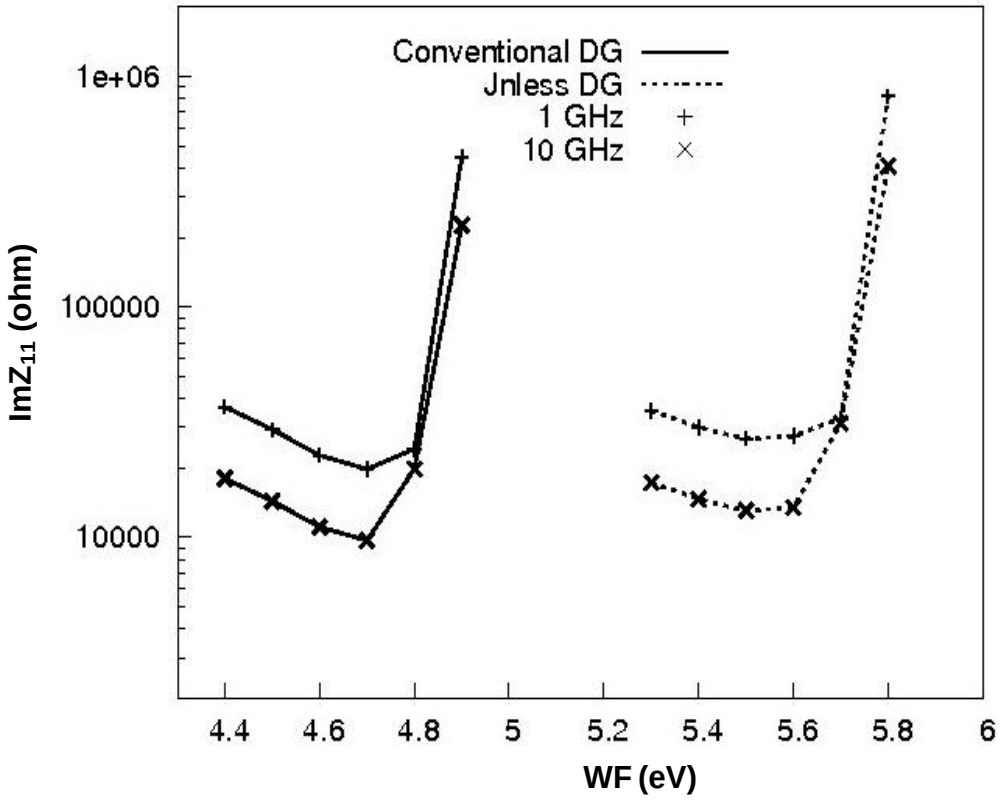

Figure 11. Variation of Imaginary part of Z_{11} w.r.t WF for conventional and junctionless DG.

REFERENCES

Choi SJ, Moon D, Kim S, Duarte JP, Choi YK (2011).Sensitivity of threshold voltage to Nanowire Width Variation in Junctionless Transistors. IEEE Elect. Dev. Lett. 32(2):125-127.

Colinge JP, Lee CW, Ferain I, Akhavan ND, Yan R, Razavi P, Yu R, Nazalov AN, Doria RT (2010b). Reduced electric field in junctionless transistors. Appl. Phys. Lett. 96(7).

Colinge JP, Lee CW, Afzalian A, Akhavan ND, Yan R, Ferain I, Razavi P, O' Neill B, Blake A, White M, Kelleher AM, McCarthy B and Murphy R (2010a). Nanowire transistors without junctions. Nat. Nanotechnol. 5:225-229.

Colinge JP, Lee CW, Afzalian A, Dehdashti N, Yan R, Ferain I, Razavi P, Neil BO, Blake A, White M, Kelleher AM, Mccarthy B, Murphy R (2009). SOI gated resistor: CMOS without junctions. Proceedings of SOI IEEE conference held at Foster City, CA. pp. 1-2.

Doria RT, Pavanello MA, Trevisoli RD, Souza M, Lee CW, Ferain I, Akhavan ND, Yan R, Razavi P, Yu R, Kranti A, Colinge JP (2011). Junctionless Multiple-Gate Transistors for Analog Applications. IEEE Trans. Elect. Dev. 58(8):2511-2519.

Hwang CH, Li Y, Han MH (2010). Stasitical Variability in FinFET devices with intrinsic parameter fluctuations. Micro Elect. Reliab. 50(5):635-638.

Hwang CH. Li TY, Han MH, Lee KF, Cheng HW, and Li Y (2009). Statistical Analysis of Metal Gate Workfunction Variability, Process Variation, and Random Dopant Fluctuation in Nano-CMOS Circuits Proceedings of 14th International Conference on Simulation of Semiconductor Processes and Devices, (SISPAD) held at San Diego, CA. pp. 99-102.

Kang CY, Choi R, Song SC, Ju BS, Hussain MM, Lee BH, Yang JW, Zeitzoff P, Pham D, Xiong W, Tseng HH (2006). Effects of ALD TiN Metal Gate Thickness on Metal Gate/High-k Dielectric SOI FinFET Characteristics. Proceedings of IEEE International SOI Conference held at Niagara Falls, NY. pp. 135-136.

Kranti A, Armstrong GA (2007). Design and Optimization of FinFETs for Ultra-Low-Voltage Analog Applications. IEEE Trans. Elect. Dev. 54(12):3308-3316.

Lee CW, Borne A, Ferain I, Afzalian A, Yan R, Akhavan ND, Razavi P, Colinge JP (2010c). High-Temperature Performance of Silicon Junctionless MOSFETs. IEEE Trans. Elec. Dev. 57(3):620-625.

Lee CW, Ferain I, Afzalian A, Yan R, Akhavan ND, Razavi P, Colinge JP (2010b). Performance estimation of junctionless multigate transistors. Solid State Electr. 54(2):97-103.

Lee CW, Nazarov AN, Ferain I, Akhavan ND, Yan R, Razavi P, Yu R, Doria RT, and Colinge JP (2010a). Low subthreshold slope in junctionless multigate transistors. Appl. Phys. Lett. 96(1).

Leung G, Chui CO (2011). Variability of inversion mode and Junctionless FinFETs due to Line Edge Roughness. IEEE Electr. Dev. Lett. 32(11):1489-1491.

Luan DH, Alshareef HN, Harris HR, Wen HC, Choi K, Senzaki Y, Majhi P, Leed BH (2006). Evaluation of titanium silicon nitride as gate electrodes for complementary metal-oxide semiconductor. Appl. Phy. Lett. 88(4).

Ponton D, Palestri P, Esseni D, Selmi L, Tiebout M, Parvais B, Siprak D, Knoblinger G (2009). Design of Ultra-Wideband Low-Noise Amplifiers in 45-nm CMOS Technology: Comparison Between Planar Bulk and SOI FinFET Devices. IEEE Trans. Circuits Systems-I. 56(5):920-932.

Souza M, Pavanello MA, Trevisoli RD, Doria RT, Colinge JP (2011).Cryogenic Operation of Junctionless Nanowire Transistors. IEEE Elect. Dev. Lett. 32(10):1322-1324.

Synopsys Sentaurus Device User Guide, 2008-2009.