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Full Length Research Paper

High voltage buried step-doping p+ layer silicon-on-insulator lateral double diffused mosfet (SOI LDMOSI) with a back-gate

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A high voltage buried step-doping p+layer (BSP+L) lateral double diffused mosfet (LDMOS) on silicon-on-insulator (SOI) with a back-gate is proposed. The new structure is characterized by a BSP+L on the buried oxide under the source. When a high positive bias is applied to the back-gate in the off-state, the depleted BSP+L greatly enhances the electric field in the buried oxide layer under the source. Compared with conventional SOI LDMOS, much higher vertical breakdown voltage is sustained by the buried oxide layer under the source. Moreover, the reduced surface electric field (RESURF) effect is enhanced by the BSP+L, resulting in improvement of lateral breakdown voltage. Simulation results show that breakdown voltage of the new structure is improved greatly while on-resistance is relatively low.

Key words: Silicon-on-insulator, breakdown voltage, back-gate, buried step-doping p+ layer.

INTRODUCTION

The advantages of silicon-on-insulator (SOI) technology attract much attention in smart power integrated circuits which are applied widely in communications and consumer electronics (Farzad and Hossein, 2010). However, vertical breakdown voltage of SOI LDMOS is difficulty to improve due to limitation of thickness silicon and buried oxide layers (Hu et al., 2011). Many structures are proposed to improve the vertical breakdown voltage, which are all applied at zero back-gate bias. There are some effective methods, enhancing the electric field in the buried oxide layer (Nakagawa et al., 1991; Hu and Luo, 2010), sharing the breakdown voltage with substrate (Tadikonda et al., 2004; Orouji et al., 2009; Luo et al., 2010; Luo et al., 2010), and so on. In some cases, the back-gate bias of SOI LDMOS is not zero, such as SOI LDMOS used in a serial connection (Schwantes et al., 2005). It is reported that breakdown voltage can benefit from a proper positive back-gate bias (Schwantes et al., 2005; Wang et al., 2009; Qiao et al., 2007). A concept of SOI back-gate reduced bulk field (BG REBULF) is proposed too (Qiao et al., 2007). However, a large positive back-gate bias weakens the reduced surface field (RESURF) effect, leading to a low breakdown voltage and large on-resistance (Schwantes et al., 2005).

To further improve the breakdown voltage and trade-off between breakdown voltage and on-resistance, a high voltage buried step-doping p+ layer (BSP+L) LDMOS on silicon-on-insulator with a back-gate (BSP+L BG SOI) is proposed. The BSP+L can enhance the electric field in the buried oxide layer under the source and reduce that at the source surface. Therefore, a high breakdown voltage is obtained without a large on-resistance.

STRUCTURE AND MECHANISM

The cross-section of the BSP+L BG SOI is showed in Figure 1, in which a BSP+L is inserted between the SOI and buried oxide layers at the source side. The BSP+L is averagely divided into n regions. P_i is the doping concentration of i region of the BSP+L and $\Delta=c\times P_1$, where c is a positive constant. P_i decreases gradually by Δ from i=1 to n. L_P and t_P are the length and thickness of BSP+L, respectively. The x axis represents the lateral distance from the left edge of the structure and the y axis represents the vertical distance from the SOI layer surface.

For a proper positive back-gate bias, the vertical breakdown

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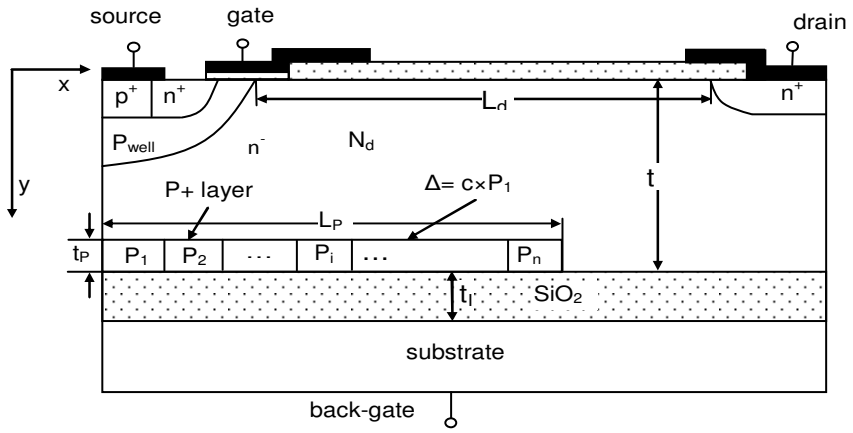

Figure 1. Schematic cross-section of the BSP+L BG SOI.

voltage of SOI LDMOS is sustained by the depletion and buried oxide layers under the source and drain due to the modulation of bulk electric field in silicon (Qiao et al., 2007). If the breakdown voltage is only limited by the vertical breakdown voltage, the maximum breakdown voltage (BV) can be approximately expressed by:

$$BV = V_{DBG} + V_{BG} \quad (1)$$

where V_{DBG} refers to the voltage drop from the drain to back-gate and V_{BG} refers to the back-gate bias. This means that breakdown voltage can be improved by only increasing V_{BG}. However, it is difficult to further improve the breakdown voltage of conventional SOI LDMOS at a larger positive back-gate bias because of weakness of the RESURF effect. Figure 2 shows the equipotential contours of the new structure and conventional SOI LDMOS at their own maximum breakdown voltages which are obtained by optimizing the back-gate biases and other parameters. Equipotential contours of the BSP+L BG SOI distribute much more in the buried oxide under the source than those of conventional SOI LDMOSI. So the corresponding electric field is much higher than that of conventional SOI LDMOS as well. The electric field (E_I) can be expressed by:

$$E_I = (\varepsilon_S E_S + Q_S)/\varepsilon_I \quad (2)$$

where E_S is the electric field on the bottom interface of the BSP+L, Q_S is charge density of the depleted BSP+L. and ε_S and ε_I are the permittivities of Si and SiO_2, respectively. After the thin BSP+L is depleted fully, a high negative density (Q_S) layer is formed and E_S is enhanced significantly. Therefore, E_I is greatly enhanced by Q_S and E_S. Before the breakdown occurs, V_{BG} is higher than that of conventional SOI LDMOS. The increment of the breakdown voltage is approximately equals to the increment of V_{BG}. Moreover, the BSP+L and drift region form a vertical junction and it shares space charge in the drift region with the lateral P_{well}/n^- junction. As a result, the RESURF effect is enhanced and on-resistance is reduced.

SIMULATION RESULTS AND DISCUSSION

Figure 3 gives the lateral and vertical electric field distributions of BSP+L BG SOI and conventional SOI LDMOSI at the difference breakdown voltages and back-gate biases. When a positive bias 120 V is applied to the back-gate of conventional SOI LDMOS, the surface electric field is increased at the source and drift region due to the modulation of electric field, as shows in Figure 3A. The breakdown voltage of the conventional SOI LDMOS is 459 V at V_{BG}=120 V, which is 35.39% higher than that at V_{BG}=0 V. For the new structure, the BSP+L can not only reduce the surface electric field at the source but also enhance that at the drift region. A uniform surface electric field is obtained and the lateral breakdown voltage is further increased, when compared with conventional SOI LDMOS. Figure 3B gives the vertical electric field distributions of the BSP+L BG SOI and conventional SOI LDMOSI. As a result of the same distributions of the three vertical electrical fields at the drain, their V_{DBG} are equal. However, the E_I is enhanced greatly by the BSP+L at the source. It is increased from about 2.7×10^5 V/cm of the conventional SOI LDMOS at back-gate bias 120 V to above 1.6×10^6 V/cm of the BSP+L BG SOI at back-gate bias 380 V and breakdown voltage from 459 to 710 V. As aforementioned, the increment of the breakdown voltage is almost equal to increment of V_{BG}.

Figure 4 gives the influences of the BSP+L parameters on breakdown voltage. A step-doping concentration profile in the BSP+L is adopted for higher breakdown voltage. When n=0, the BSP+L BG SOI is conventional SOI LDMOS. The maximum breakdown voltage increases with increase of n from 0 to 10, but is saturated at n=10, as shows in Figure 4a. The maximum breakdown voltage 710 V is obtained at n=10, V_{BG}=380 V, which is higher by 54.68% than that of the conventional SOI LDMOS at n=0, V_{BG}=120 V. Figure 4B gives the influences of L_P on the breakdown voltage of the BSP+L BG SOI. The back-gate bias is optimized for the maximum breakdown voltage. At first, the maximum breakdown voltage increases with increase of L_P, due to the enhancement of E_I and RESURF effect. And then the maximum breakdown voltage decreases, because more

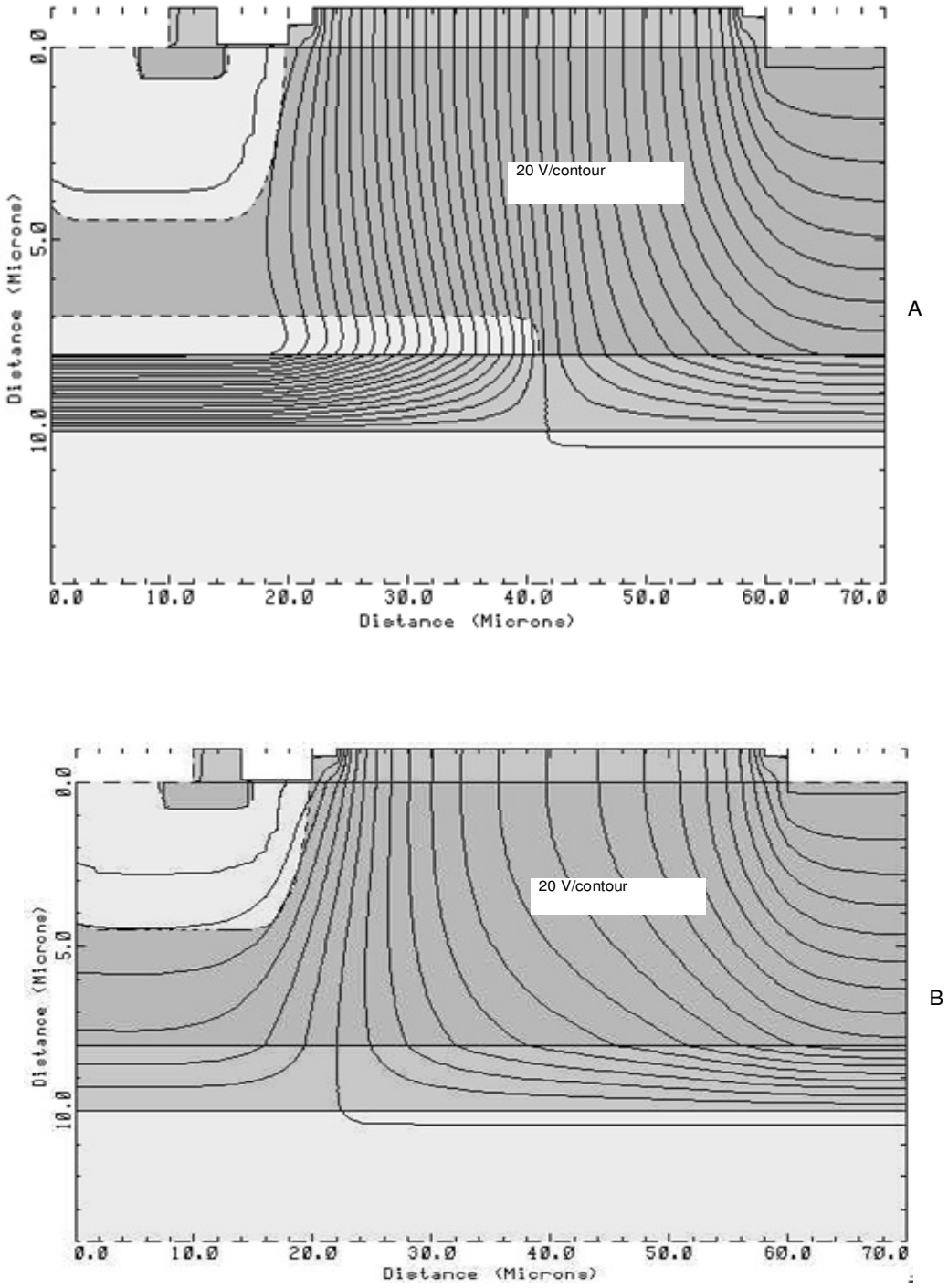

Figure 2. Equipotential contours of the BSP+L BG SOI and conventional SOI LDMOS at breakdown (L_d=40 μm, t_S=8 μm and t_I=2 μm). A, BSP+L BG SOI (N_d=1.4 × 10^{15} cm^{-3}, t_P=1 μm, L_P=40 μm, n=10, P_1=1.8×$10^{17}$$cm^{-3}$, Δ=-0.085$P_1$, V_{BG}=380 V and BV=710 V); B, Conventional SOI LDMOSI (N_d=1.2 × $10^{15}$$cm^{-3}$, V_{BG}=120 V and BV=459 V).

equipotential contours concentrate at the end of BSP+L with increase of L_P resulting in the premature breakdown. Table 1 compares the specific on-resistance of the BSP+L BG SOI and the SOI LDMOSI, which are optimized for certain breakdown voltages and back-gate biases. The specific on-resistance of the BSP+L BG SOI is lower than that of the conventional SOI LDMOS at the same breakdown voltage because the RESURF effect is

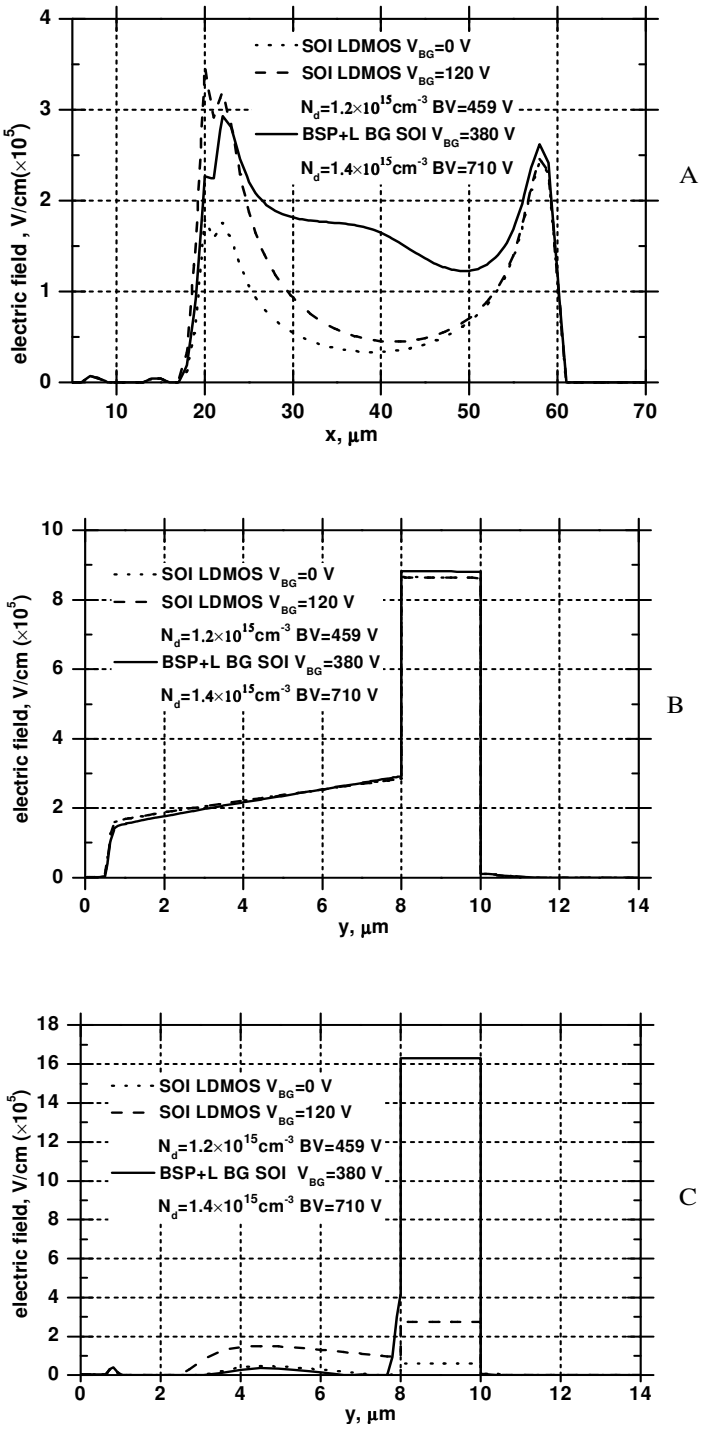

Figure 3. Lateral and vertical electric field distributions of BSP+L BG SOI and conventional SOI LDMOS (L_d=40 μm, t_S=8 μm, t_I=2 μm, t_P=1 μm, L_P=40 μm, n=10, P_1=1.8 × 10^{17}cm^{-3}, Δ=-0.085P_1). A, Lateral field distributions (y=0.1 μm); B, Vertical electric field distributions at the drain side (x=69.9 μm); C, Vertical electric field distributions at the source side(x=8 μm).

enhanced by BSP+L. Even if the breakdown voltage of the new structure is improved greatly, the specific on-resistance is not increased significantly. The specific on-resistances is 8.37 Ω.mm^2 when the breakdown voltage

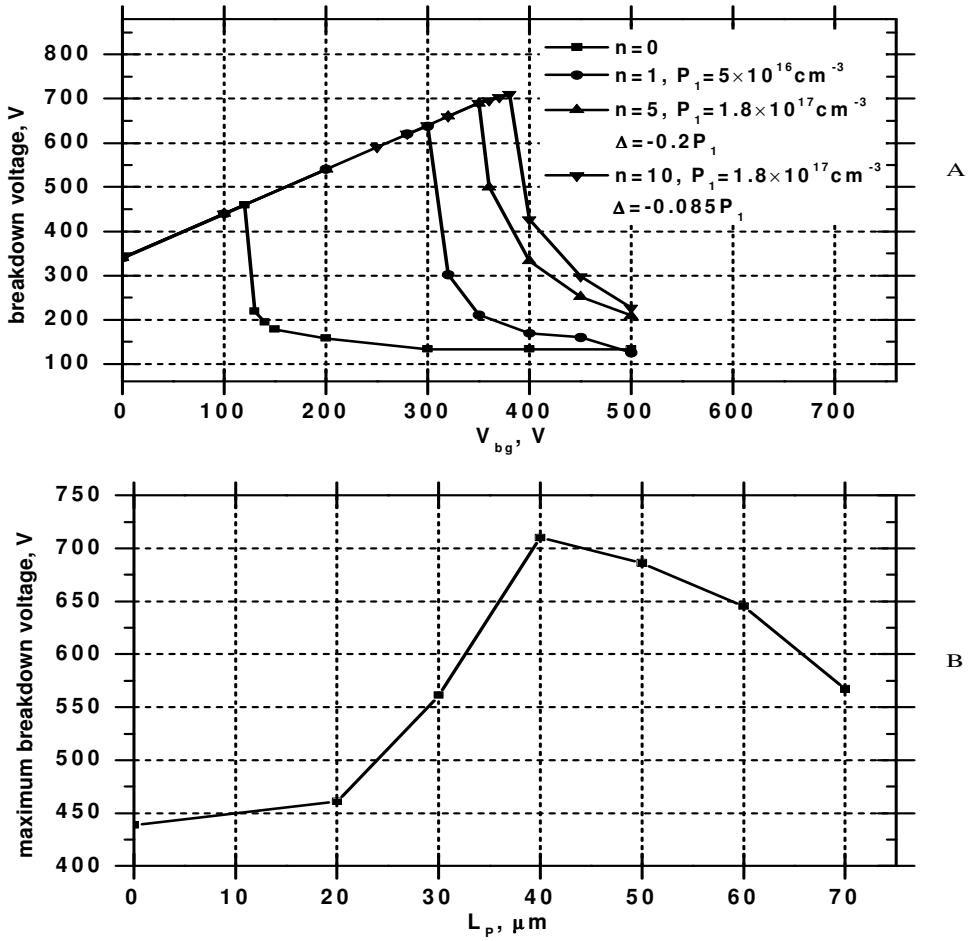

Figure 4. Influences of BSP+L parameters on breakdown voltage of BSP+L BG SOI and conventional SOI LDMOSI with difference back-gate voltages (L_d=40 μm, t_S=8 μm, t_I=2 μm and t_P=1 μm). A, Influence of n on breakdown voltage (L_P=40 μm); B, influence of L_P on breakdown voltage (n=10, P_1 and Δ are optimized for breakdown voltage).

Table 1. Compares of specific on-resistances of the BSP+L BG SOI and SOI LDMOSI.

Structure	BSP+L BG SOI	BSP+L BG SOI	SOI LDMOSI
Back-gate voltage /V	380	120	120
Breakdown voltage /V	710	459	459
concentration of the drift cm^{-3}	1.4×10^{15}	2.5×10^{15}	1.2×10^{15}
Specific on-resistance /Ω.mm^2	8.37	7.23	7.44
Length of drift region /μm	40	40	40

is 710 V.

Conclusion

The BSP+L BG SOI is proposed. The BSP+L can enhance the electric field in the buried oxide under the source and reduce that at the source surface. With relatively low on-resistance, the breakdown voltage of the new structure is 710 V, which is twice of the breakdown voltage of the conventional SOI LDMOS.

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