

*Full Length Research Paper*

# Efficient enhancement of polymer light emitting diode by inserting hole blocking layer

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Accepted 18 January, 2011

**The triplet layer for the PLED was fabricated with ITO / PVK (77 nm) / CdS (115 nm) / Alq<sub>3</sub> (84 nm) / Al (300 nm). The PLED devices were inserted in the CdS layer between the 77 nm PVK and 84 nm Alq<sub>3</sub> absorbing the ambient light to reduce the reflection of the device. The maximum wavelength and luminescence intensity increase with the thickness of CdS. This indicated that the maximum wavelength shifted to a higher wavelength when the thickness of CdS increases. With the insertion of 115 nm of CdS layer between the PVK and Alq<sub>3</sub>, a lower turn on voltage can be obtained at 5.4 eV.**

**Key words:** Cadmium sulphide, photoluminescence, energy band gap, electrical conductivity, optical reflectance.

## INTRODUCTION

In 1990, a Cambridge group of friends announced a conduction of polymer-based LED (PLED) involving aromatic,  $\pi$  conjugated species. The field of PLEDs has grown rapidly and has now entered industrialization. This new field has recorded enormous progress made in the improvements of color gamut, luminance efficiency and device reliability. The organic systems and the polymeric materials in particular, have the distinctive advantages that are easy to process.

In 1990, Burroughes et al. (1999) reported a very-high-efficiency green-light-emitting polymer LEDs (PLEDs) with conjugated polymer of poly (p-phenylene vinylene) (PPV) shown in Figure 2. The device used PPV as a precursor coated on the ITO by ion beam sputtering. Aluminum (Al) worked as a cathode by thermal evaporation. Since then, the conjugated polymer has been given considerable attention and intensive studies have been done on the PLEDs. Braun and Heeger from the University of California at Santa Barbara have an

interest in the electroluminescence from conjugated polymer materials.

Further study in PLEDs has focused more on phosphorescent emissive materials, like Iridium complexes such as Tris [2-(p-tolyl) pyridine] and Iridium (III) [Ir (mppy)<sub>3</sub>]. The electrophosphorescence converts the electrical energy in an OLED into light in a highly efficient manner (Kang et al., 2007; Tsutsui et al., 1999). The internal quantum efficiency of the devices has been improved to approximately 25% by using these phosphorescent materials. This is due to the decay radioactivity of both the singlet and triplet excitons compared to a standard PLED, where only the singlet states will contribute to emission of light.

Recently, a number of researches have been carried out by using organic materials as hole blocking layers, such as: N, N'-dicarbazolyl-4,4'-biphenyl (Peng et al., 2006), bathcuproine (Ikai et al., 2001; Adachi et al., 2001; Kwong et al., 2001; Kolosov et al., 2002), 4-biphenylphenolate aluminium (III) bis (2-methyl-8-quinolino-4-phenylphenolate (Kim et al., 1999; Jae et al., 2007), 1,8-naphthalimides (Vadim et al., 2003) and polyquinolines (Chandra et al., 1980). A good example is seen in devices reported by Jae et al. (2007), where

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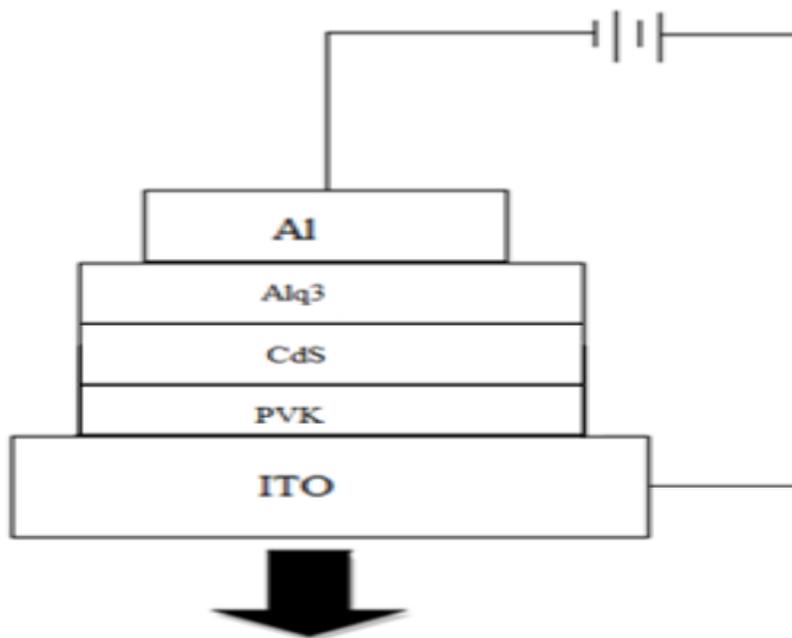


Figure 1. The structure of OLED device.

silane and triazine moieties, 2,4-diphenyl-6-(49-triphenylsilanyl)biphenyl-4-yl)-1,3,5-triazine (DTBT) were used as hole blocking materials, and N,N'-dicarbazolyl-4,4'-biphenyl (CBP) doped with *fac*-tris(2-phenylpyridine) iridium [ $\text{Ir}(\text{ppy})_3$ ] showed a maximum external quantum efficiency of 17.5% with a maximum power efficiency of  $47.8 \text{ lm W}^{-1}$ . The insertion of the HBL will solve the problem of excitons leakage, in which efficiency blocks the diffusion of holes from the luminescent layer into the ETL layer (Alex et al., 2004).

Cadmium sulfide is in the hexagonal structure and it has a direct band gap semiconductor with a band gap of 2.42 eV. It has useful properties for optoelectronics, being used in both photosensitive and photovoltaic devices. Thin films of CdS are required in components, such as a photoresistor and solar cells (Eih-Zhe et al., 2003), nonlinear integrated optical devices and light emitting diodes (LEDs) or laser heterostructures for emission in the visible spectral range (Johnson et al., 1995; Peng et al., 2006). It has been reported that some research used CdS nano particles as a active layer for light emission (Ikai et al., 2001). Chemically synthesized cadmium sulfide (CdS) nano particles are deposited on Si substrate and they exhibit electroluminescence, corresponding to different process treatment. Thus, optimum thickness of the CdS is very important to improve the performance of the OLEDs. Therefore, in this paper, the effect of CdS thickness is reported on the electrical conductivity, turn on voltage and photoluminescence of the CdS as a hole

blocking layer in OLED device.

## EXPERIMENTALS

In this experiment,  $\text{Alq}_3$  was used as the ETL and PVK as the HTL, while Indium Tin Oxide (ITO) was used as the anode aluminium (Al) and cathode, respectively. Devices with a structure of ITO / PVK (77 nm) / CdS (T nm) /  $\text{Alq}_3$  (84 nm) / Al (300 nm) were fabricated, where T was chosen as 75, 90, 105, 115 and 134 nm. The PVK and  $\text{Alq}_3$  compounds were purchased from Sigma-Aldrich. The PVK was deposited on a substrate by using deep coating method to transfer it onto indium tin oxide (ITO) glass substrates with a sheet resistance of about  $15 \Omega$ , while the  $\text{Alq}_3$  and CdS were deposited by thermal evaporation at room temperature in a high vacuum chamber (Figure 1). The ITO glass was immersed in ultrasonic bath with acetone for 10 min. Then, the ITO glass was rinsed in deionized water for 10 min and then, it was blown dry with nitrogen gas. This procedure was used to remove organic contamination and particles from the ITO surface.

Current-voltage measurement was carried out using current-voltage source (Keithley, 2400). The thickness of the layers was measured by disk profile machine (Tencor P-12). The photoluminescence (PL) of the films was measured using Spectrofluorometer (Ocean Optics 2000 FLG). Spectrophotometer and Micro Autolab Type III Potentiostat were used for measuring the energy band gap and cyclic voltametry study.

## RESULTS AND DISCUSSION

Figure 3 showed that the different thicknesses of CdS were inserted between the PVK and  $\text{Alq}_3$  to enhance the

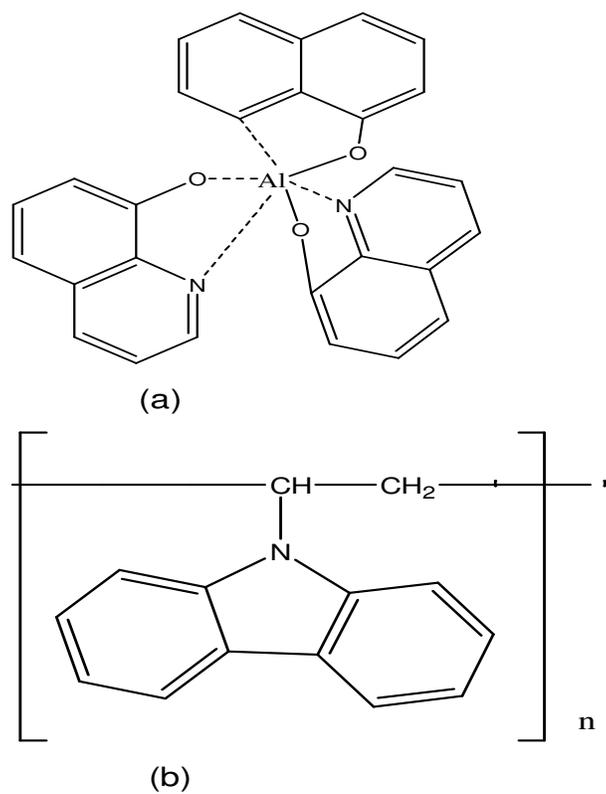


Figure 2. Molecular structure of (a) Alq<sub>3</sub> and (b) PVK.

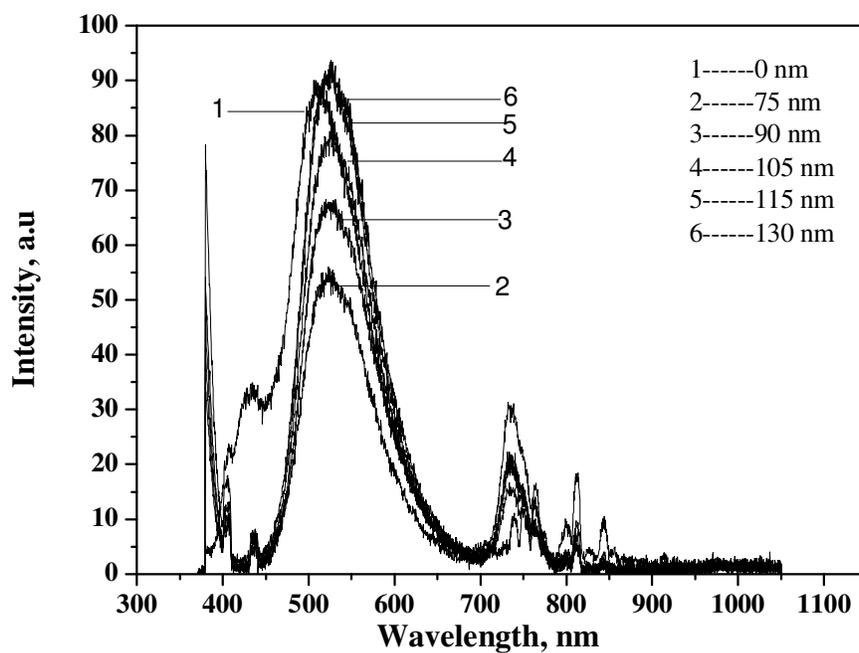
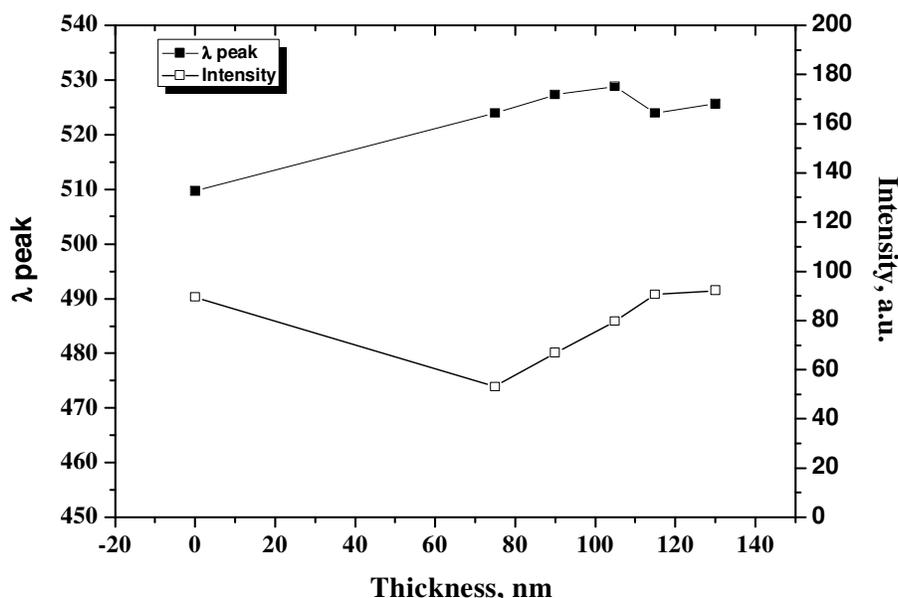


Figure 3. Photoluminescence spectrum for different thickness of CdS with 77 nm PVK and 84 nm Alq<sub>3</sub>.



**Figure 4.**  $\lambda$  peak versus intensity for different thickness of CdS with 77 nm PVK and 84 nm Alq<sub>3</sub>.

luminescence intensity of the PLED devices. Triplet layers of PLED devices were prepared with ITO / PVK (77 nm) / CdS (T nm) / Alq<sub>3</sub> (84 nm) / Al (300 nm), where T was chosen as 75, 90, 105, 115 and 130 nm. The maximum wavelength for the PLED device, without the CdS layer, was around 530 nm. However, the maximum wavelength shifted to a higher wavelength (550 nm), when the CdS was inserted between the PVK and Alq<sub>3</sub>. This may be due to the fact that the PVK can be used as a light emitting layer in the PLED device, while the 550 nm is attributed to the excimer emission of PVK. The relationship between the  $\lambda$  peak and the luminescence intensity for the triplet layers PLED is shown in Figure 4. The maximum wavelength and luminescence intensity increase with the thickness of CdS. This indicated that the maximum wavelength shifted to a higher wavelength, when the thickness of CdS increased. When the film was excited by 345 nm light, the maximum emission was observed at 550 nm, confirming an efficient energy transfer from the PVK excimer to CdS. As a result, Forster-type energy transfer is expected to occur at the interface of PVK and CdS. In addition, the hole transport barrier between the host PVK and the CdS blocks holes, directly quenches at the cathode, hence increasing the probabilities of charge trapping and recombination on the emitting layer, which leads to high efficiency.

This is very important to minimize the reflectance of the PLED, but also to simultaneously maximize its emission through the optimization of its transmittance. The PLED devices insert the CdS layer between the 77 nm PVK and

the 84 nm Alq<sub>3</sub>, which absorb the ambient light to reduce the reflection of device. From Figures 5 and 6, the CdS with 115 nm has the lowest intensity reflectance light which is 6 a.u. The reduction of the reflectance of the device is done by introducing an insertion of the layer between the HTL and ETL. This is an approach that can also enhance the extraction of light from the device since CdS is a good photoconductivity which absorbs light.

Figure 7 shows the I-V characterization for the different thickness of CdS insertion between the PVK and Alq<sub>3</sub>. The thicknesses of the CdS are from the range of 75 to 130 nm. It can be found that the current initially increase with the increase of CdS thickness until 105 nm. This implies that once the CdS molecules are introduced into the devices, the CdS molecules will trap the hole and reduced the mobility of the hole. Further increase in the thickness of the CdS, until 115 nm, shows a decrease in the trend of the current. There are some pre-trapped electrons in the emitting layer, when the voltage applied to the electron helps the injection of the hole into the emitting layer. Thus, with higher CdS thickness, the number of trapped electrons increased.

To determine the turn-on voltage of each multi layer PLED devices, the corresponding Fowler-Nordheim plot  $\log(I/V^2)$  versus  $1/V$ , in Figure 8, yields a straight line which implies that the measured anode current follows the model of Fowler-Nordheim model and can be defined as a field emission current. Generally, field emission is characterized using the theory of Fowler and Nordheim. Figure 9 showed that the turn-on voltage without the

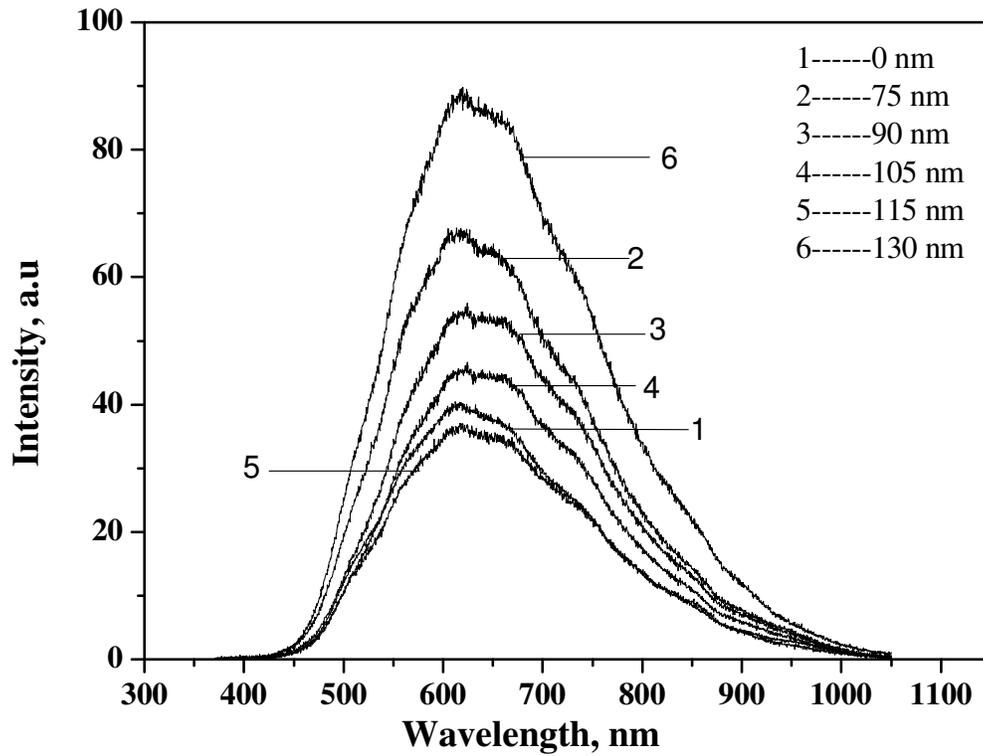


Figure 5. The reflectance light for different thickness of CdS with 77 nm PVK and 84 nm Alq<sub>3</sub>.

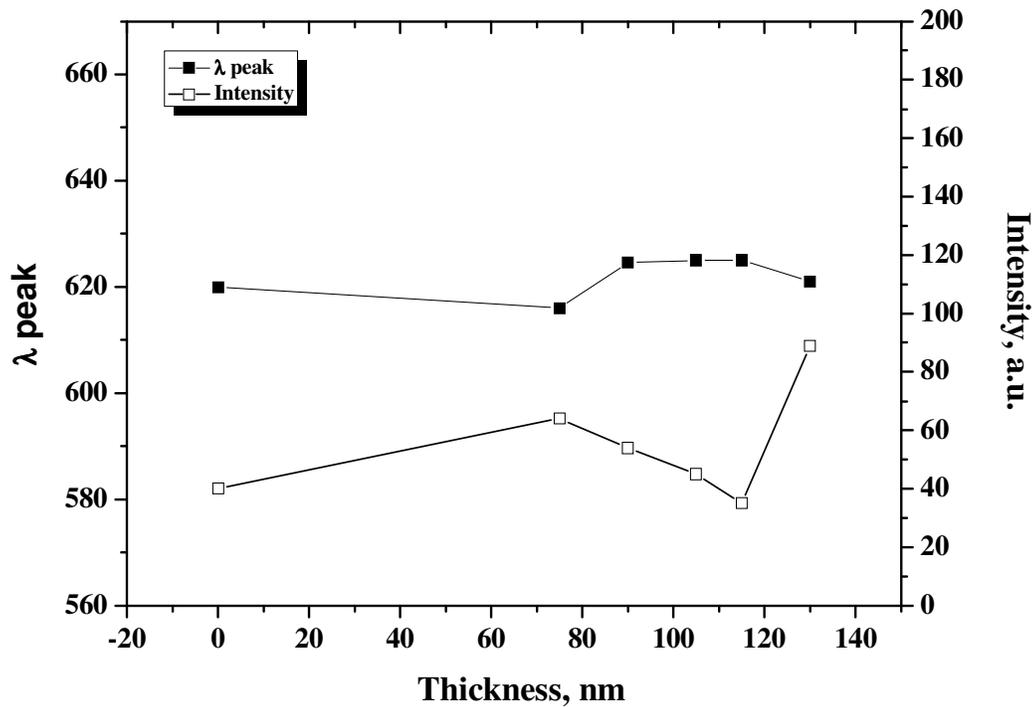
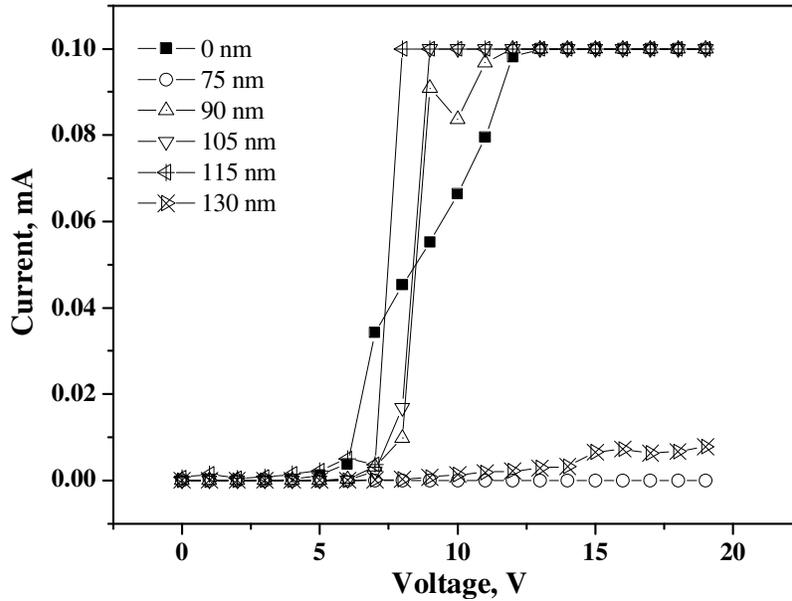
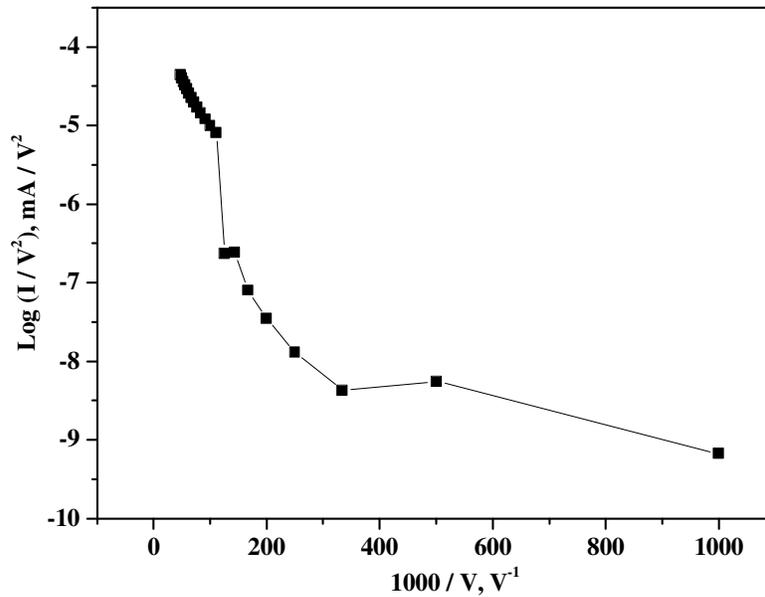


Figure 6. The reflectance light for different thickness of CdS with 77 nm PVK and 84 nm Alq<sub>3</sub>.



**Figure 7.** I-V characteristic for different thickness of CdS with 77 nm PVK and 84 nm Alq<sub>3</sub>.

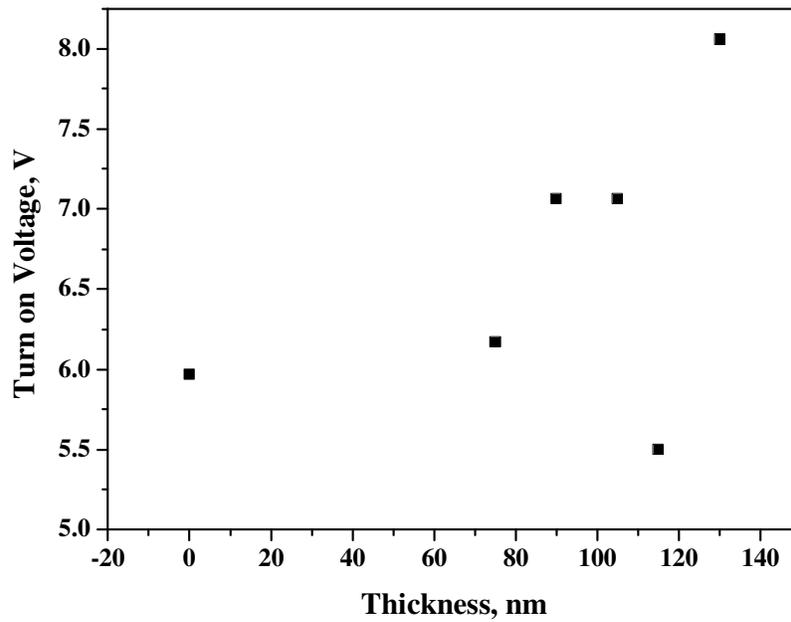


**Figure 8.** The corresponding Fowler-Nordheim plot for 84 nm Alq<sub>3</sub>, 115 nm CdS and 77 nm PVK PLED device.

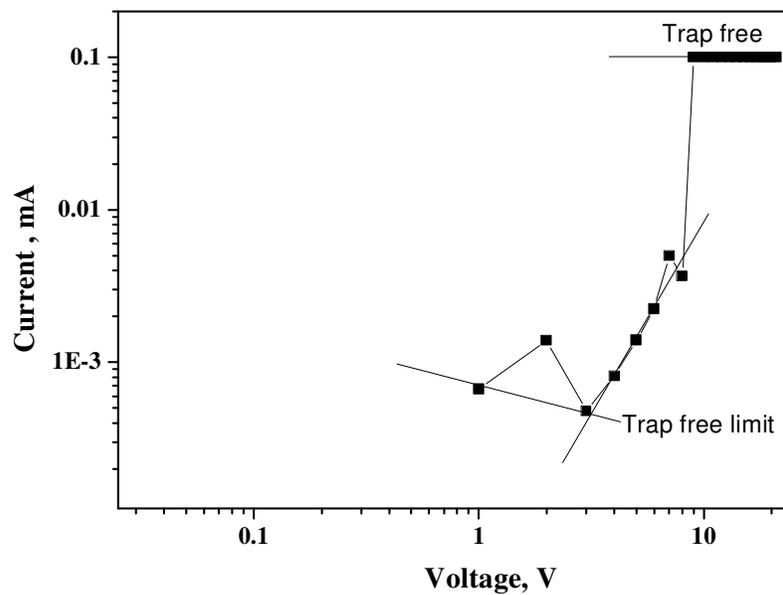
CdS layer is 5.9 V; however, by inserting 115 nm of CdS layer between PVK and Alq<sub>3</sub>, a lower turn-on voltage can be obtained at 5.4 V. The decrease in the turn-on voltage is due to the decrease in the trap density which means lower voltage is required to send the electron to interface

PVK: Alq<sub>3</sub>. As a conclusion, the optimum thickness of CdS will enhance the injection of the hole.

Figure 10 depicts the log-log scale I-V characteristics of the multi layers PLED devices with the 84 nm Alq<sub>3</sub>, 115 nm CdS and 77 nm PVK. The I-V curve shows three



**Figure 9.** Turn-on voltage for OLED devices with different thickness of CdS with 77 nm PVK and 84 nm Alq<sub>3</sub>.



**Figure 10.** I-V characteristic on a log-log scale for the devices with 84 nm Alq<sub>3</sub>, 115 nm CdS and 77 nm PVK PLED.

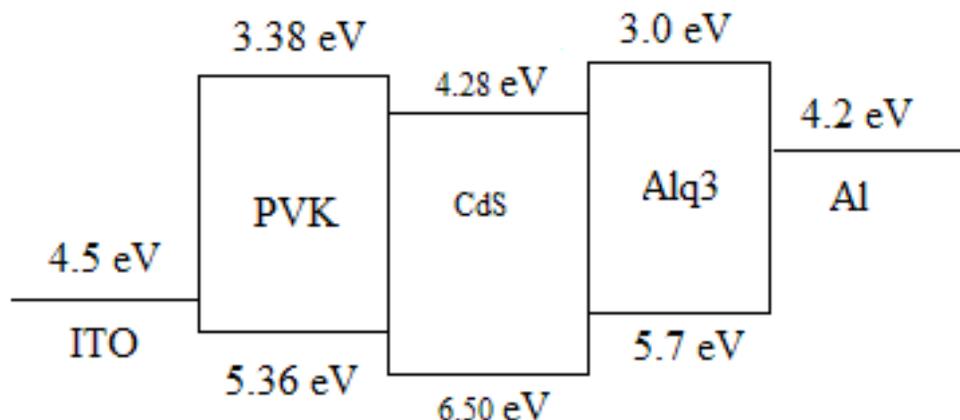
distinct regions, characteristic of a one-carrier single set of traps. These regions include:

(1) The Ohmic region, where the current density is

proportional to the voltage;

(2) SCLC trap limited region;

(3) Trap-filled limit, where the onset trap-filled voltage (VTFL) results in the density of traps; and



**Figure 11.** Energy band diagram of ITO / NPB (55 nm) / CdS (115 nm) / Alq<sub>3</sub> (84 nm) / Al (300 nm) device.

(4) The final region, in which the current is only limited by the space charge and is free from the influence of traps.

With the CdS layer found in the electric field region, where only a part of the deep traps become filled, the increase of current with increasing electric field is fast, resulting in the power law dependence with a power larger than 2. This is the so-called trap-filled limited region, where ionic defects can create the relevant deep-trap energy levels in the band gap.

To improve the efficiency of the PLED, inserting a layer between the HTL and ETL is needed in order for the luminescence values to result at a low current density. Figure 11 shows a proposed energy level diagram of the PLED device.

The lower HOMO level of CdS (6.50 eV), than those of Alq<sub>3</sub> and PVK, leads to better confinement of holes within the emitting layer. This is due to the efficient electron injection from the ETL into the emitting layer. The mobility electron in the material is higher and it increases the quantum efficiency of the device. This is in good agreement with the findings of the literature, which stipulates that the quantum efficiency improves if a material with high triplet energy and low HOMO level is used as the HBL.

## Conclusions

The OLEDs with the ITO/ PVK (77 nm) / CdS (130 nm) / Alq<sub>3</sub> (84 nm) /Al have been successfully fabricated using thermal evaporation and dip coating method. The device with 115 nm of CdS produces the lowest current turn-on voltage which is 5.4 V and gives the highest intensity of the light emission.

## ACKNOWLEDGEMENTS

The authors gratefully acknowledge the financial support received from Malaysia Government through Fundamental Research Fund (FRGS 01-11-08-664FR/5523664). More so, Mei Yee is grateful for the financial support of NSF scholarship (2009 to 2010).

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