

Full Length Research Paper

Development of the 3-phase 4-wire voltage sag generator

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This paper presents development of 3-phase 4-wire voltage sag generator. Voltage sag generator is based on 3-phase 4-wire inverter in order to handle the neutral current caused by the unbalance and non-linear load. The controller used for this voltage sag generator is a low-cost dsPIC microcontroller. The 3 kVA voltage sag generator has been implemented. The paper also describes software to simulate and create controlled signal for generator. Software allows the user to directly program the voltage sag waveform by selecting the sag magnitude, sag duration, phase shift and voltage sag type. The simulation and experimental results have shown that this voltage sag generator can generate voltage sag in any conditions.

Key words: Voltage sag generator, 3-phase 4-wire inverter, low-cost dsPIC.

INTRODUCTION

A recent survey found that 92% of all disturbances in a power system are caused by voltage sags. An electrically sensitive load often trips or shuts down when voltage sag occurs. It is very important to know how such sensitive equipment works when voltage sag occur. A voltage sag generator is able to create various types of voltage sag waveforms. Voltage sag can be classified into seven types as described by Bollen (2000).

Previous works (Takahashi et al., 2008; Rylander et al., 2007; Bhavar et al., 2008; Teke et al., 2008; Ma and Karady, 2008) have developed voltage sag generator which can be simply classified into 4 types. These four types of voltage sag generator are transformer, switching-impedance, generator and amplifier. The transformer type uses a switch to adjust both pre-sag voltage and sag magnitudes. The switching-impedance type creates voltage sags by switching impedance into a power system by using a thyristor-controlled reactor

(TCR). The generator type uses a synchronous generator to give controlled 3-phase voltage sags. The amplifier type uses a waveform generator to create controlled 3-phase voltage sags.

An autotransformer is used as the 1-phase voltage sag generator as demonstrated by Rylander et al. (2007) and Bhavar et al. (2008). Rylander et al. (2007) used MOSFET to turn-on/turn-off for changing between the primary source and the secondary source. Bhavsar et al. (2008) used motorized variac with multi tapping transformer, the position of the variac is changed using a signal generated by the microcontroller PIC (Peripheral Interface Controller). The main disadvantage of this method is that the non-conducting pairs connected to the unselected taps dissipate power due to the taps. It has a complex structure and requires control of signal processors. The TCR type creates a difference in voltage by firing the TCR at different angles. The disadvantages of TCR are the generation of low frequency harmonic current components and higher losses when working in the inductive region (Teke et al., 2008). The generator type uses a synchronous generator that provides voltage sag by changing the exciting current of the generator. The control of sag generator's operation and monitoring of the system under test in is performed by the Visual Basic programming (Collins and Morgan, 1996). The

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Abbreviations: TCR, Thyristor-controlled reactor; RP, region pointer; GUI, graphic user interface; PWM, pulse width modulation; LC, lumped element; USB, universal serial bus.

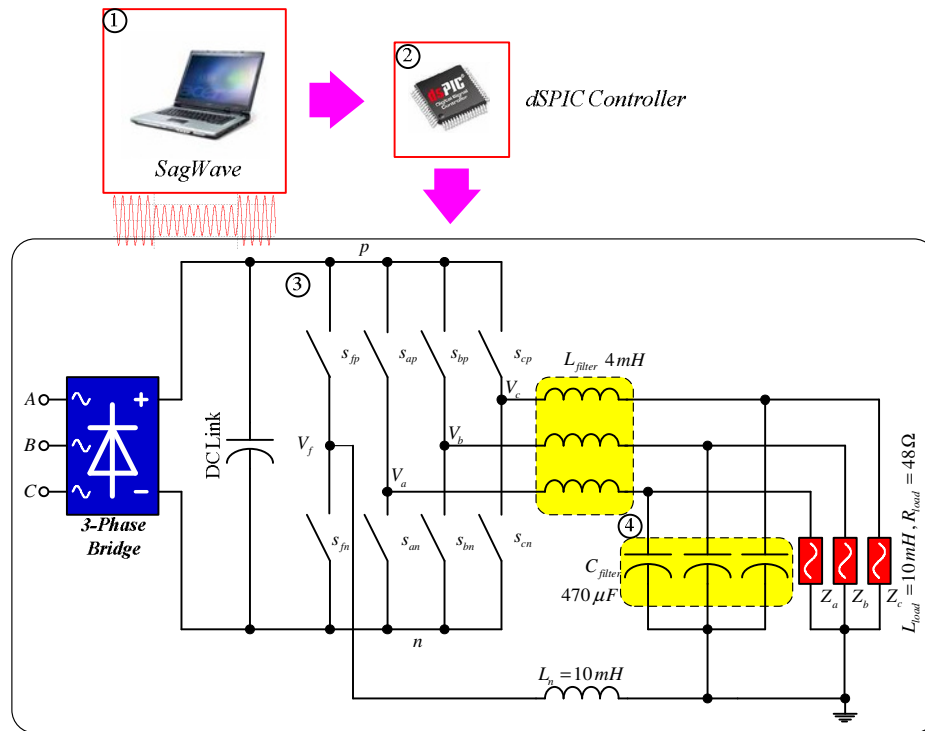


Figure 1. The proposed 3-phase 4-wire voltage sag generator prototype.

software of this paper had not displayed the waveform of voltage sag, and disadvantages of this type are that, it needs more space to install and it is expensive (Ma and Karady, 2008). The amplifier type can provide voltage sags with varying magnitude, duration, frequency and harmonics. After defining the desired waveform data is passed to power amplifier, at which outputs of adequate voltage levels of voltage sag are produced. This type is more convenient than others types, because it enables more precise control of all voltage sag characteristics and also allows testing of equipment in context of frequency variations and harmonic distortions. Therefore, a power amplifier type of voltage sag generator is selected for designing the voltage sag generator in this study. This paper presents a 3-phase 4-wire voltage sag generator based on an abc algorithm.

The 3-phase 4-wire voltage sag generator

Voltage sag generator is based on 3-phase 4-wire inverter in order to handle the neutral current caused by the unbalance and non-linear load. The configuration of 3-phase 4-wire voltage sag generator is shown as block diagram in Figure 1. The voltage sag generator prototype consists of a 3-phase 4-leg 4-wire inverter, graphic user interface (GUI) waveform generator, a dsPIC controller, and low pass filter. The details of each part are described as following:

A 3-phase 4-leg 4-wire inverter

The main advantage of 3-phase 4-leg 4-wire inverter is its ability to deal with load unbalance in a system. The goal of 3-phase 4-leg 4-wire inverter is to maintain the desired sinusoidal output voltage waveform for all loading conditions. The neutral connection is presented to handle the ground current due to unbalanced loads (Oranpiroj et al., 2005). The 3-phase 4-leg 4-wire can responses to the unbalance voltage and unbalance current, the fourth leg of inverter allows the circulation of the neutral current.

The 3-phase 4-leg 4-wire inverter is shown in Figure 2. The addition of a fourth leg extends the space vectors from two to three dimensions, making the selection of the modulation vectors complex (Zhan et al., 2002). In recent years, the 3-phase 4-leg 4-wire inverter has used three-dimensional space vector modulation techniques (Zhan et al., 2001). Three-dimensional space vector modulation uses a representation of voltage vectors in $\alpha\beta\gamma$ coordinates (Zhan et al., 2003). However, three-dimensional representation of the switching vectors in $\alpha\beta\gamma$ is difficult to understand. Most methods based on $\alpha\beta\gamma$ representation need to determine the “sextant” in which the desired voltage vector is included, which leads to many complicated operations, including rotations. Avoiding the traditional $\alpha\beta\gamma$ transformation, the space vector modulation algorithm in abc coordinates presented by Parales et al. (2003) can simplify, by the selection of

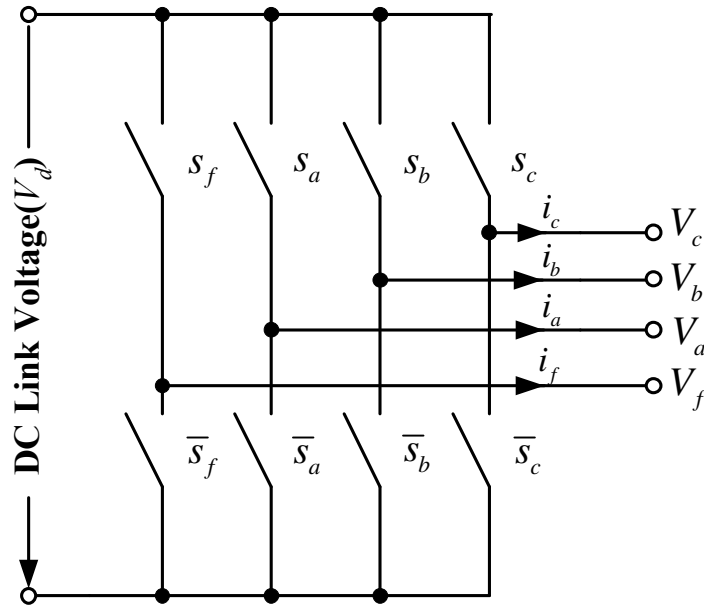


Figure 2. 3-phase 4-leg 4-wire voltage source inverter.

Table 1. Switching state, output voltage and switching vector.

Stage	s_f	s_a	s_b	s_c	V_{af}	V_{bf}	V_{cf}	Vector
1	0	0	0	0	0	0	0	V1
2	0	0	0	1	0	0	1	V2
3	0	0	1	0	0	1	0	V3
4	0	0	1	1	0	1	1	V4
5	0	1	0	0	1	0	0	V5
6	0	1	0	1	1	0	1	V6
7	0	1	1	0	1	1	0	V7
8	0	1	1	1	1	1	1	V8
9	1	0	0	0	-1	-1	-1	V9
10	1	0	0	1	-1	-1	0	V10
11	1	0	1	0	-1	0	-1	V11
12	1	0	1	1	-1	0	0	V12
13	1	1	0	0	0	-1	-1	V13
14	1	1	0	1	0	-1	0	V14
15	1	1	1	0	0	0	-1	V15
16	1	1	1	1	0	0	0	V16

switching vectors and the calculation of duty cycles reducing the complexity of the modulation algorithm. Therefore, the 3-phase 4-leg 4-wire inverter with three-dimensional space vector modulation (3D-SVM) in this study is based on an abc algorithm (Parales et al., 2003; Oranpiroj et al., 2009).

The abc 3D-SVM algorithm reference is obtained in the abc coordinates, it will not be necessary to change into $\alpha\beta\gamma$ coordinates. The line-neutral voltage (V_{af}, V_{bf}, V_{cf})

are given by:

$$V_{if} = [s_i - s_f] \cdot V_d \quad (1)$$

where: $i = a, b, c$

The output voltage vector and its coordinates are shown in Table 1. Where s_a, s_b, s_c, s_f are switching

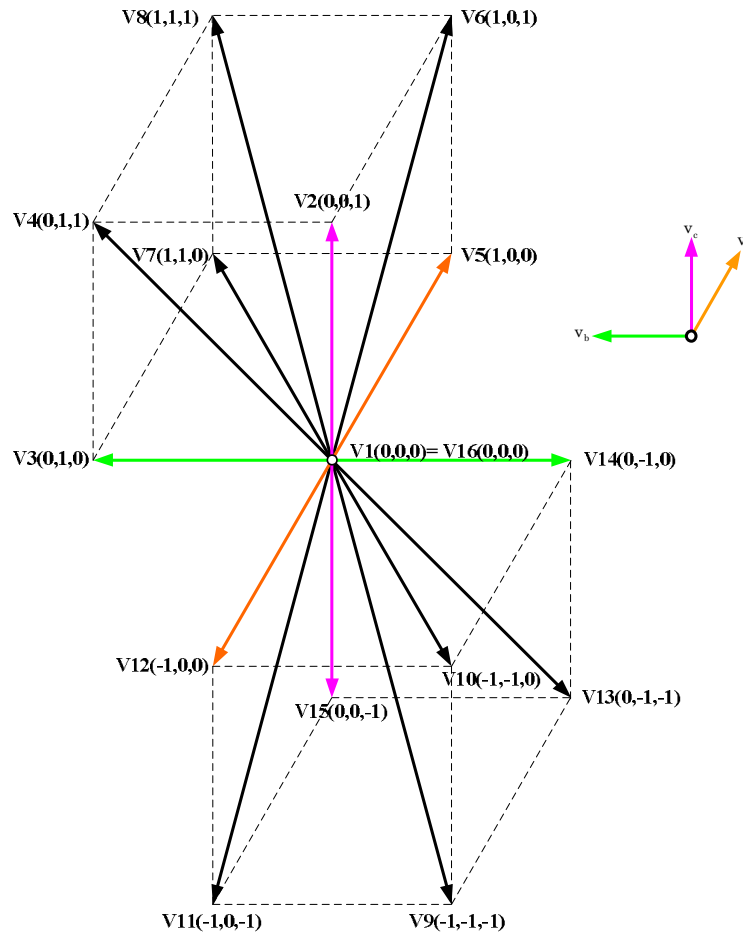


Figure 3. Switching vectors based on abc coordinate.

combinations, (upper switch is turned on = 1, upper switch is turned off = 0). Where V_{af}, V_{bf}, V_{cf} are line to neutral voltage with normalized by dc-link voltage (V_d).

The 3D switching vectors are located in two cubes, with an edge length of 1: one of them is placed in the “all positive” region of the space defined (vectors 1 – 8) and the other in the “all negative” region (vectors 9 – 16), as represented in Figure 3.

This space containing 24 tetrahedron, each one is formed by three nonzero switching vector and two zero vectors. The method of determination of this tetrahedron in which the reference vector is located was proposed by Parales et al. (2003). The possible tetrahedrons which can be used by the switching vectors are limited to 24 tetrahedrons; the selected tetrahedron is determined by a region pointer (RP) which is defined by:

$$RP = 1 + \sum_{i=1}^6 C_i g^{(i-1)} \tag{2}$$

where:

$$C_i = \text{Sign}\left(\text{INT}\left(x(i) + 1\right)\right) \quad i = 1:6 \tag{3}$$

The calculation of the region pointer according to the space vector modulation theory is done by comparing the positive and negative relationships among the 3-phase reference voltages V_{af}, V_{bf}, V_{cf} . We obtain (Wu et al., 2005):

- If $V_{af} > 0$, then $C_1 = 1$, else $C_1 = 0$,
- If $V_{bf} > 0$, then $C_2 = 1$, else $C_2 = 0$,
- If $V_{cf} > 0$, then $C_3 = 1$, else $C_3 = 0$,
- If $V_{af} - V_{bf} > 0$, then $C_4 = 1$, else $C_4 = 0$,
- If $V_{bf} - V_{cf} > 0$, then $C_5 = 1$, else $C_5 = 0$,
- If $V_{af} - V_{cf} > 0$, then $C_6 = 1$, else $C_6 = 0$.

Table 2. Duty cycle calculation, region pointer, non-zero switching vectors.

RP	Vd1	Vd2	Vd3	d1	d2	d3
1	V9	V10	V12	$-V_{cf}$	$V_{cf} - V_{bf}$	$V_{bf} - V_{af}$
5	V2	V10	V12	V_{cf}	$-V_{bf}$	$V_{bf} - V_{af}$
7	V2	V4	V12	$V_{cf} - V_{bf}$	V_{bf}	$-V_{af}$
8	V2	V4	V8	$V_{cf} - V_{bf}$	$V_{bf} - V_{af}$	V_{af}
9	V9	V10	V14	$-V_{cf}$	$V_{cf} - V_{af}$	$V_{af} - V_{bf}$
13	V2	V10	V14	V_{cf}	$-V_{af}$	$V_{af} - V_{bf}$
14	V2	V6	V14	$V_{cf} - V_{af}$	V_{af}	$-V_{bf}$
16	V2	V6	V8	$V_{cf} - V_{af}$	$V_{af} - V_{bf}$	V_{bf}
17	V9	V11	V12	$-V_{bf}$	$V_{bf} - V_{cf}$	$V_{cf} - V_{af}$
19	V3	V11	V12	V_{bf}	$-V_{cf}$	$V_{cf} - V_{af}$
23	V3	V4	V12	$V_{bf} - V_{cf}$	V_{cf}	$-V_{af}$
24	V3	V4	V8	$V_{bf} - V_{cf}$	$V_{cf} - V_{af}$	V_{af}
41	V9	V13	V14	$-V_{af}$	$V_{af} - V_{cf}$	$V_{cf} - V_{bf}$
42	V5	V13	V14	V_{af}	$-V_{cf}$	$V_{cf} - V_{bf}$
46	V5	V6	V14	$V_{af} - V_{cf}$	V_{cf}	$-V_{bf}$
48	V5	V6	V8	$V_{af} - V_{cf}$	$V_{cf} - V_{bf}$	V_{bf}
49	V9	V11	V15	$-V_{bf}$	$V_{bf} - V_{af}$	$V_{af} - V_{cf}$
51	V3	V11	V15	V_{bf}	$-V_{af}$	$V_{af} - V_{cf}$
52	V3	V7	V15	$V_{bf} - V_{af}$	V_{af}	$-V_{cf}$
56	V3	V7	V8	$V_{bf} - V_{af}$	$V_{af} - V_{cf}$	V_{cf}
57	V9	V13	V15	$-V_{af}$	$V_{af} - V_{bf}$	$V_{bf} - V_{cf}$
58	V5	V13	V15	V_{af}	$-V_{bf}$	$V_{bf} - V_{cf}$
60	V5	V7	V15	$V_{af} - V_{bf}$	V_{bf}	$-V_{cf}$
64	V5	V7	V8	$V_{af} - V_{bf}$	$V_{bf} - V_{cf}$	V_{cf}

The calculation of the duty cycle can be expressed as:

$$d = M_d^{-1} V_{ref} \quad (4)$$

where

$$V_{ref} = \begin{bmatrix} V_{cf} \\ V_{bf} \\ V_{af} \end{bmatrix}, \quad d = \begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix}, \quad M_d = \begin{bmatrix} Vd1_a, Vd2_a, Vd3_a \\ Vd1_b, Vd2_b, Vd3_b \\ Vd1_c, Vd2_c, Vd3_c \end{bmatrix}$$

The duty cycles of the zero vector are calculated as $d_0 = 1 - d_1 - d_2 - d_3$. Based on a minimum harmonic

criterion, the switching vectors are distributed symmetrically along the middle of the switching period. The duty cycle calculations imply only addition or subtraction of reference vector components, as detailed in Table 2.

Graphic user interface (GUI) waveform generator

The GUI "SagWave" (Oranpiroj et al., 2010) is designed for easy input of the designed waveform as shown in Figure 4. The user can create sag magnitude, sag duration, phase angle jump and point on wave for a designed sag waveform from the front panel of GUI. Users can verify the desired waveform in time domain or vector form as shown in windows. Then, parameters of desired sag waveform can be sent to dsPIC

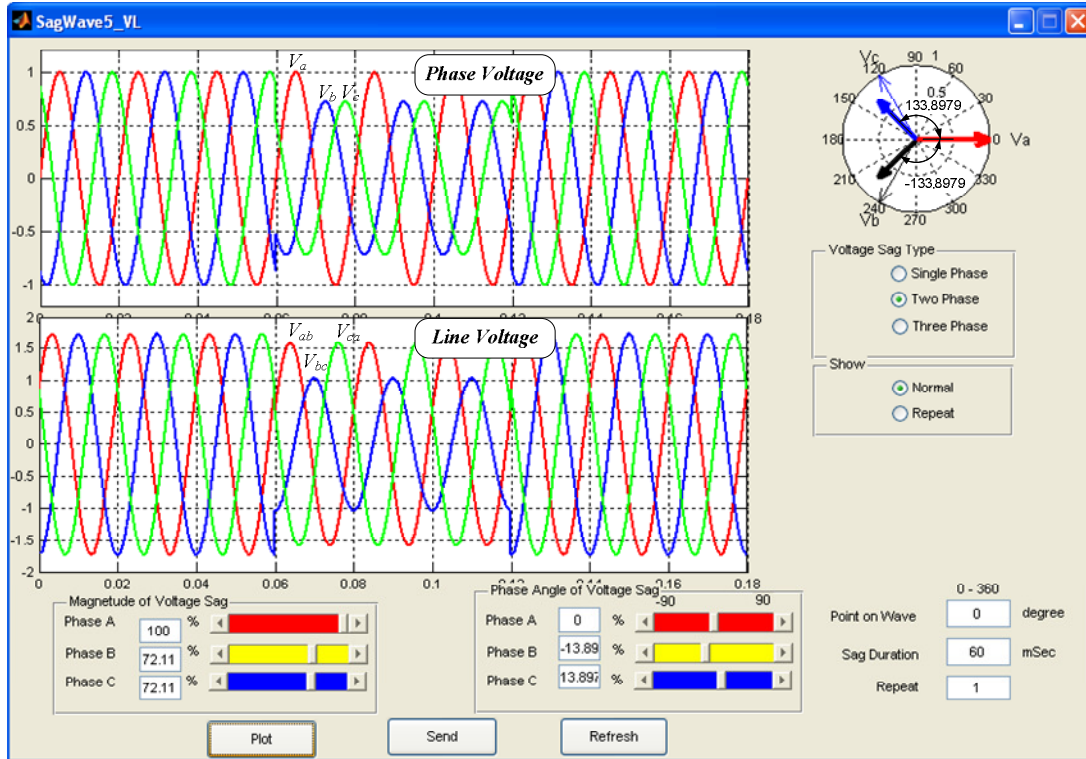


Figure 4. GUI waveform generator for creating and verifying sag type C_a waveform.

microcontroller directly from GUI to control voltage sag generator. For example, the type C of voltage sag designed waveforms by Equation 5 (Bollen, 2000).

$$\left. \begin{aligned} V_a &= 1 \\ V_b &= -\frac{1}{2} - \frac{1}{2} jV\sqrt{3} \\ V_c &= -\frac{1}{2} + \frac{1}{2} jV\sqrt{3} \end{aligned} \right\} \quad (5)$$

In this case two voltages V_b and V_c drop in magnitude and change in phase angle (phase-angle jump). In Equation 5 V_{bc} do not had phase angle jump, this is the voltage sag type C_a . In this case V had the value between $0 < V < 1$. Figure 4 shows the 3-phases voltage with $V = 0.6, V_a = 1$ and $V_b = 0.7211\angle -133.8979^\circ, V_c = 0.7211\angle 133.8979^\circ$. Figure 4 shows V_b and V_c had phase angle jump about $\pm 13.8979^\circ$, while V_{bc} do not have phase angle jump.

The duty cycle calculations imply only addition or subtraction of reference vector components, as seen in Perales et al. (2003). Once the region pointer is obtained, the switching vector and duty cycles can be calculated directly according to the reference voltage as shown in Figure 5.

The calculation of the region pointer Equation 2 and duty cycles (d_0, d_1, d_2, d_3) according to abc algorithm (Perales et al., 2004) can be performed using GUI software as shown in Figure 6. The GUI software generates the Duty.dat files, which consist of duty cycles d_0, d_1, d_2 and d_3 as shown in Figure 7. The user clicked the "Send" button to send the Duty.dat to dsPIC microcontroller by a universal serial bus (USB) port. The data in Duty.dat files update the pulse width modulation (PWM) register (PDC1, PDC2, PDC3, PDC4) in dsPIC microcontroller. The PWM output signal in dsPIC can be generated by using center aligned modes as shown in Figure 8.

Low-cost dsPIC microcontroller

The low-cost dsPIC microcontroller dsPIC30F6010 from microchip is used as controller for 3-phase sag generator. The dsPIC30F6010 is based on 16-bit digital signal controller core delivering 30MIPs operation. The dsPIC30F6010 device has a DSP (Digital Signal Processing) engine, that all DSP instructions single 25ns cycle. They have 8 PWM output channel with complementary or independent output mode, edge and center aligned mode and 10-bit analog-to-digital converter (A/D) with 4 s/h inputs, 500 Ksps

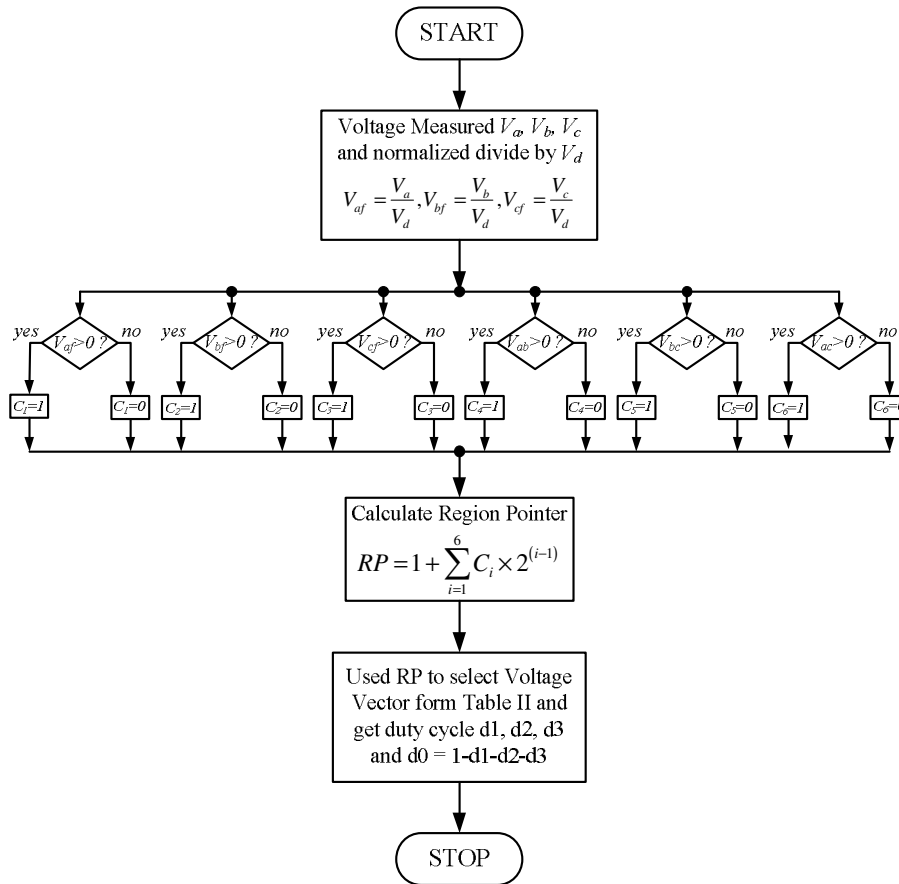


Figure 5. Flow chart of calculation of switching vector and duty cycles.

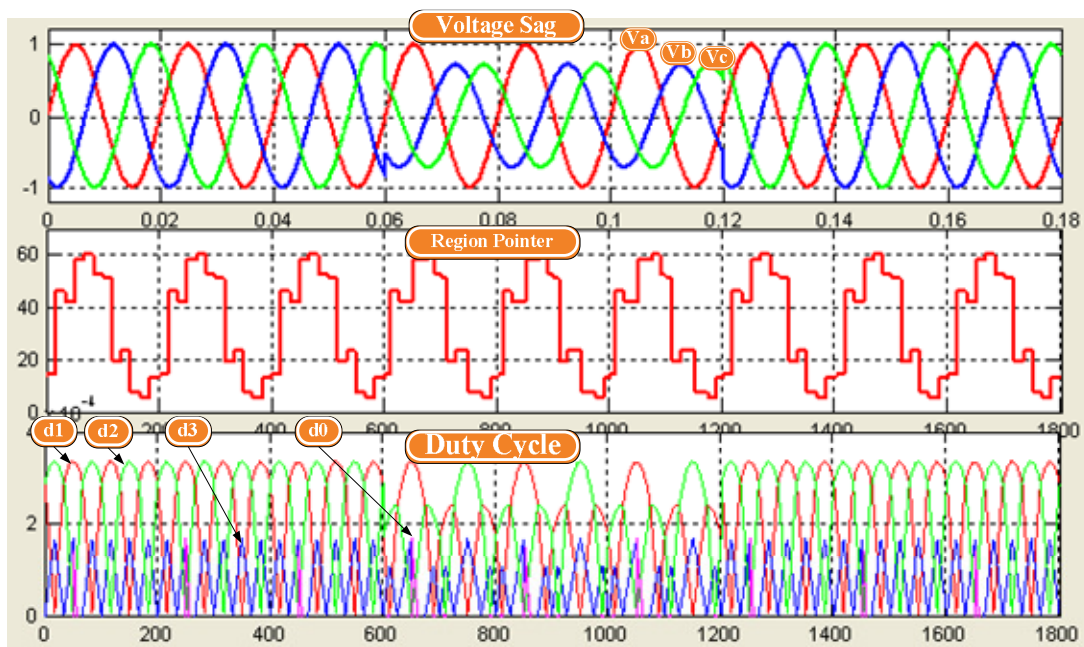


Figure 6. The region pointer and duty cycle calculated by SagWave software.

d1	d2	d3	d0
1.73E-04	1.63E-20	1.15E-04	4.46E-05
1.68E-04	2.09E-06	1.18E-04	4.58E-05
1.62E-04	4.19E-06	1.19E-04	4.73E-05
1.57E-04	6.27E-06	1.21E-04	4.90E-05
1.51E-04	8.36E-06	1.23E-04	5.10E-05
1.45E-04	1.04E-05	1.24E-04	5.34E-05
1.39E-04	1.25E-05	1.26E-04	5.59E-05
1.33E-04	1.45E-05	1.27E-04	5.88E-05
1.26E-04	1.66E-05	1.28E-04	6.19E-05
1.20E-04	1.86E-05	1.29E-04	6.53E-05
1.13E-04	2.06E-05	1.30E-04	6.90E-05
1.07E-04	2.26E-05	1.31E-04	7.29E-05
9.97E-05	2.45E-05	1.32E-04	7.71E-05
9.28E-05	2.65E-05	1.32E-04	8.16E-05
8.58E-05	2.84E-05	1.33E-04	8.63E-05
7.87E-05	3.03E-05	1.33E-04	9.12E-05

Figure 7. Data in Duty.dat files.

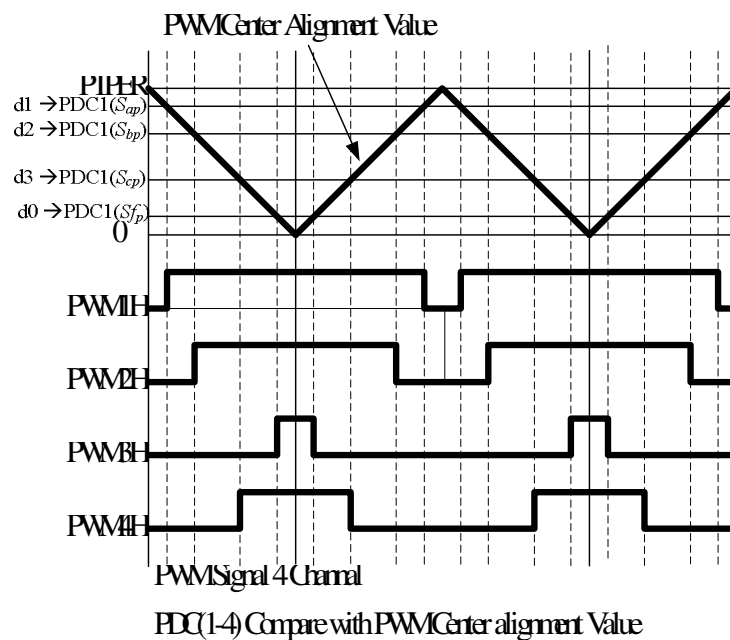


Figure 8. PWM output signal of the dsPIC.

conversion rate, 16 input channels. The features and cost of the dsPIC30F6010 make it be excellent choice for the digital control implementation of the 3-phase 4-leg 4-wire inverter. The dsPIC30F6010 microcontroller board is as show in Figure 9.

Lumped element (LC) low-pass filter

The lumped element (LC) filter is a second order filter giving -40 dB/decade over the whole frequency range. With the 3 kHz switching frequency, the resonance

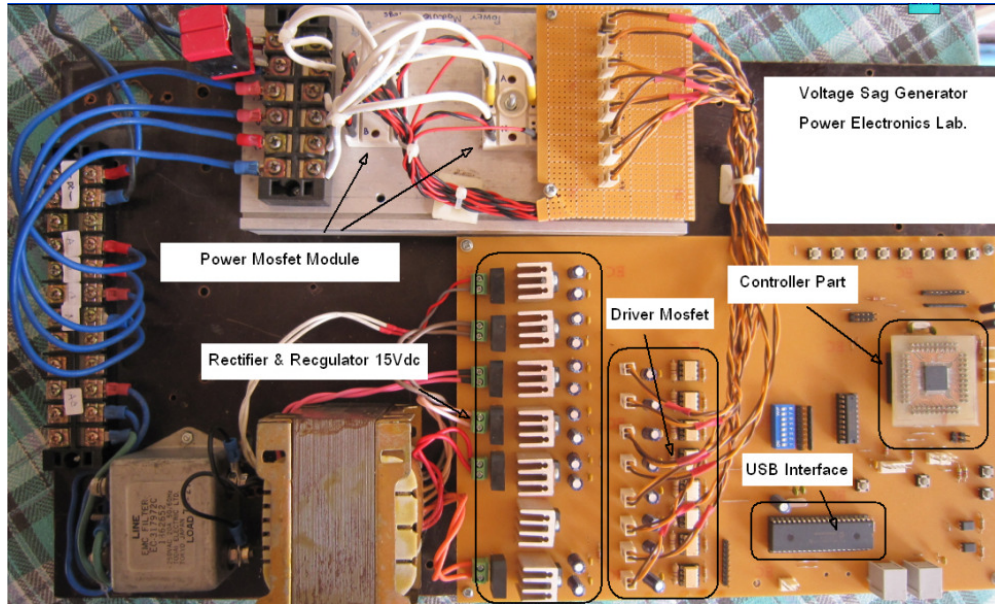


Figure 9. A dsPIC60F6010 microcontroller board and 3-phas 4-leg 4-wire inverter.

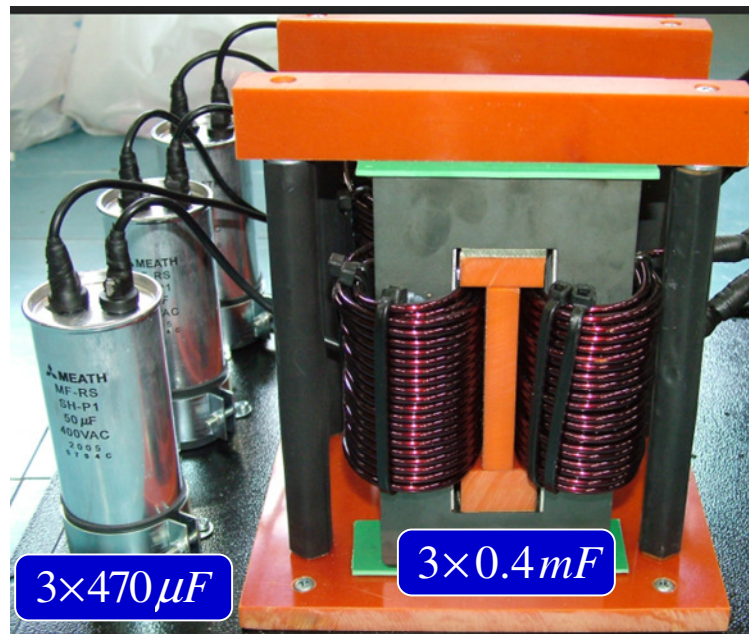


Figure 10. Low-pass LC filter.

frequency f_{res} is selected as 300 Hz to have less than 15% of voltage ripple at switching frequency. In the paper $L_f = 0.4\text{mH}$ and $C_f = 470\mu\text{F}$ were used. The resonance frequency f_{res} is:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{0.4 \times 10^{-3} \times 470 \times 10^{-6}}}$$

$$f_{res} = 367.06\text{ Hz}$$

The LC filter of this research as shown in Figure 10.

Simulation of a 3-phase 4-leg 4-wire voltage sag generator

The operation of this prototype starts with the user

Table 3. Parameters of seven types of voltage sag.

Type	Duration (ms)	Magnitude Phase A (%)	Phase (degree)	Magnitude Phase B (%)	Phase (degree)	Magnitude Phase C (%)	Phase (degree)
A	100	60	0	60	0	60	0
B	100	60	0	100	0	100	0
C	100	100	0	60	-20	60	20
D	100	60	0	100	20	100	-20
E	100	100	0	60	0	60	0
F	100	60	0	70	10	70	-10
G	100	60	0	40	-20	40	20

designing the voltage sag wave form from SagWave software. Then the user clicks the “Send” button to send the parameters to dsPIC microcontroller. The actual voltage sag is created by a 3-phase 4-leg 4-wire inverter based on an abc algorithm.

For example, the designed waveforms have parameters as found in Bollen (2000). The parameters in Table 3 are used to generate seven types of voltage sag. Users can verify waveforms through graphic display windows as shown in Figure 11.

SagWave software can create point on wave single-phase (phase A) voltage sag, the parameters are shown in Table 4. The display of waveforms was is in Figure 12. The parameters of single-phase (phase A) repeated voltage sag is shown in Table 5 and the simulation waveform in Figure 13.

Experimental 3-phase 4-leg 4-wire voltage sag generator

This segment discusses the operation of the system shown in Figure 1. The system was experimented and evaluated to learn more about the operation of the 3-phase 4-wire voltage sag generator. The system components of Figure 1 that are used in the experiment are described in Table 6. The 3 kVA 3-phase 4-leg 4-wire voltage source converter has been implemented in order to verify the operation of sag generator. The power of this prototype is limited by the converter. For this reason, the prototype is limited to a 220/380 V, 3 kVA load. However, the algorithm of sag generator controller can be applied to scaled power rating by changing to higher power rating of converter.

From the previous discussion, SagWave software generates the parameter file and sends it to the dsPIC microcontroller. The dsPIC uses this file to control the 3-phase 4-leg 4-wire inverter in order to create the actual waveform. Experimental results for voltage sag types A, B and E are shown in Figure 14 to 16, respectively.

The experimental results in Figure 14 are according with simulation results in Figure 11 (Type A). Figure 14 shows the 3-phase voltage and 3-phase current of voltage sag Type A. During voltage sag, the voltage on

phase A (V_a), phase B (V_b) and phase C (V_c) are reduced to 60%. The current on phase A (I_a), phase B (I_b) and phase C (I_c) also are reduced to 60%. Before voltage sag occurs, the neutral current (I_n) has zero currents due to the balanced load condition. However during voltage sag transition, the unbalance load currents causes non-zero in the neutral current (I_n).

The experimental results in Figure 15 are according to the simulation results in Figure 11 (Type B). Figure 15 shows the 3-phase voltage and 3-phase current of voltage sag Type B. During voltage sag, the voltage on phase A (V_a) is reduced to 60%. The current on phase A (I_a) also is reduced to 60%. Before voltage sag occurs, the neutral current (I_n) has zero currents due to the balanced load condition. However during voltage sag, the unbalance load causes an increase in the neutral current (I_n) that the return current in fourth leg of inverter.

The experimental results in Figure 16 are according to the simulation results in Figure 11 (Type E). Figure 16 shows the 3-phase voltage and 3-phase current of voltage sag Type E. During voltage sag, the voltage on phase B (V_b) and phase C (V_c) are reduced to 60%. The current on phase A (I_a) is constant, while current on phase B (I_b) and current on phase C (I_c) are reduced to 60%. Before voltage sag occurs, the neutral current (I_n) has zero currents due to the balanced load condition. However during voltage sag, the unbalance load causes an increase in the neutral current (I_n) that the return current in fourth leg of inverter.

The experimental results of point on wave are shown in Figure 17. The sag generator can generate waveform at any point of wave of sinewave as desired.

The experimental results of repeated voltage sags are shown in Figure 18. The sag generator can generate repeated voltage sag waveform as many as desired.

CONCLUSIONS

This paper has proposed the use of SagWave software to provide a visual interactive capability generating data for the dsPIC controller. SagWave software can show the waveform and the phasor of the three-phase voltage. The

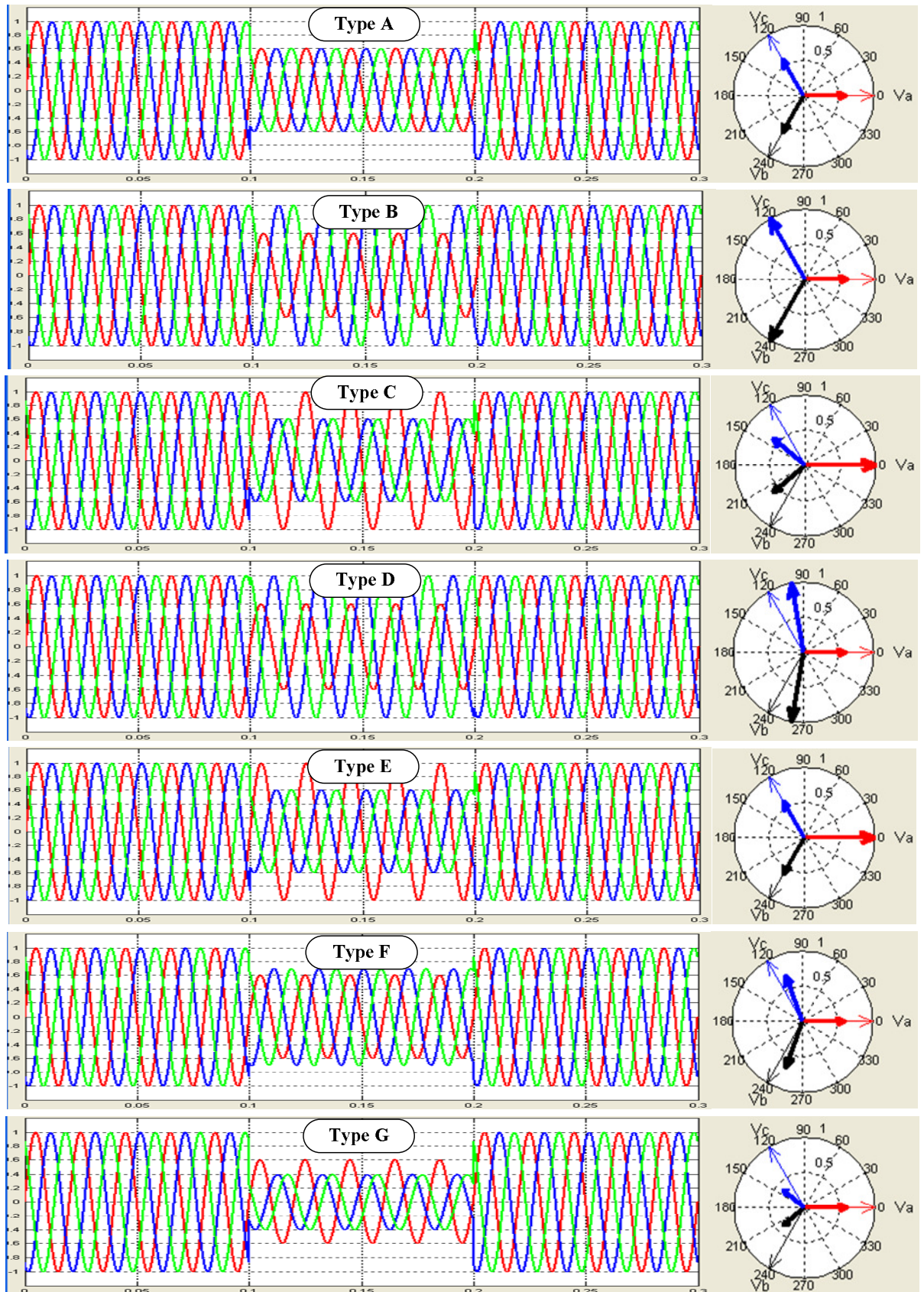


Figure 11. The seven types of voltage sag created using SagWave software.

Table 4. Parameters of point on wave voltage sag.

Case	Magnitude (%)	Duration (ms)	Point on wave (degree)
1	60	10	270
2	40	10	90
3	10	60	10

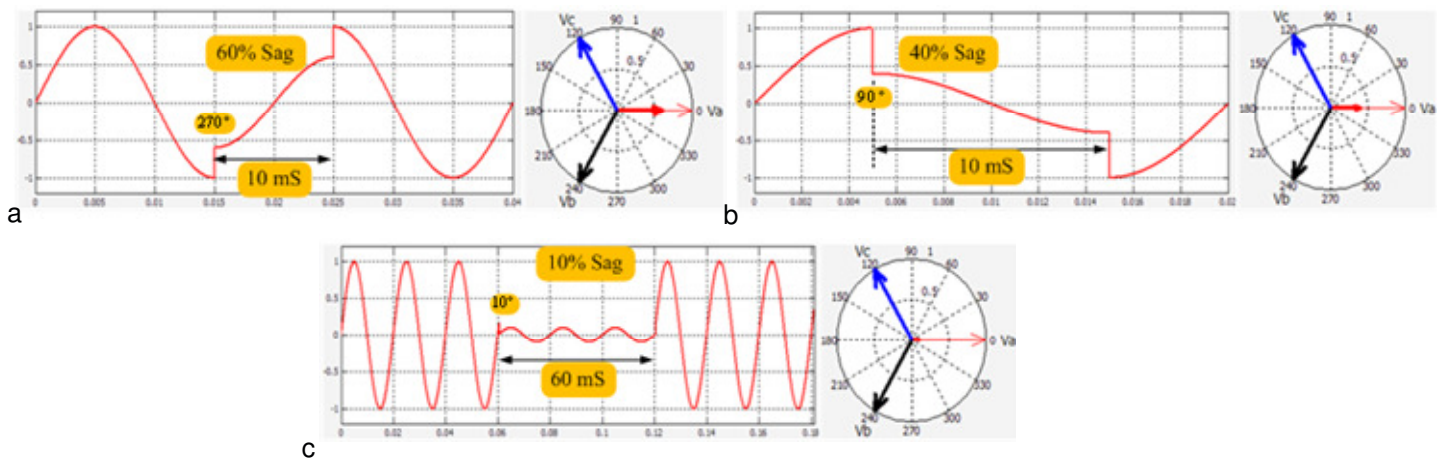


Figure 12. a, The point on wave at 270° ; b, The point on wave at 90° ; c, The point on wave at 10° .

Table 5. Parameters of repeated voltage sag.

Case	Magnitude (%)	Duration (ms)	Number of repeated
1	60	60	4
2	60	60	6

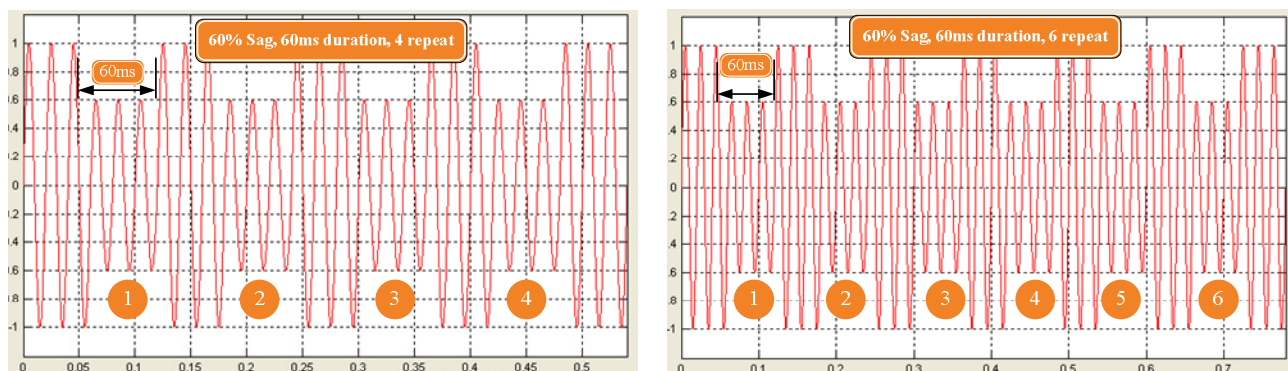


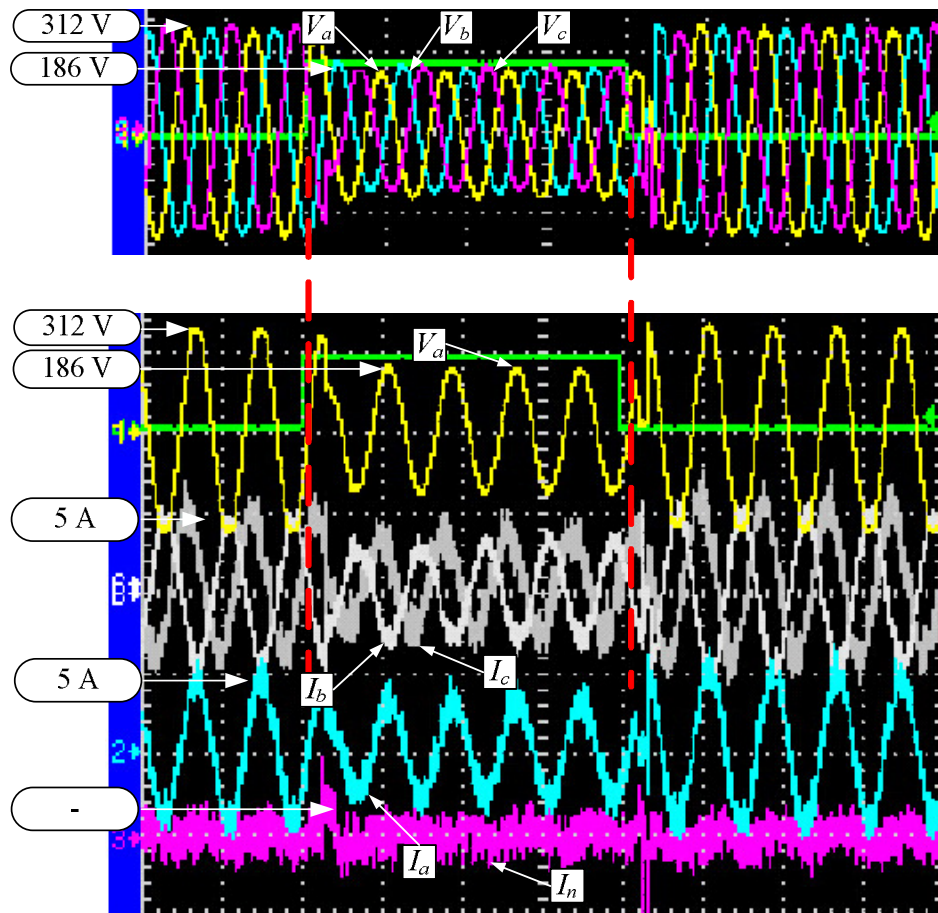
Figure 13. The simulation of single-phase voltage sag repeated.

simulation and experimental results have shown a simple control algorithm for generating the sag signal for testing.

The experimental results have shown the main advantages of this prototype: point on wave, sag

Table 6. Components used in implementing the system shown in Figure 1 for voltage sag generator.

3-Phase rectifier		3-phase 4-leg 4-wire inverter			Low pass filter		Load	
Full bridge Rectifier	Capacitor (Rectifier)	Controllable Switch	dsPIC controller	Switching frequency (f_{sw})	Filter Inductor (L_f)	Filter Capacitor (C_f)	Load Inductor (L_{load})	Load Resistor (R_{load})
37 A/600 V	3600 μF	20 A/600 V	dsPIC30F6010	3 kHz	0.4 mH	470 μF	10 mH	48 Ω

**Figure 14.** Voltage sag Type A.

duration, magnitude of voltage sag and varied type of voltage sag. The research prototype had used 3 kVA 3-phase 4-leg 4-wire voltage source converter. The power of this prototype was limited by the converter. For this reason, the prototype was limited to a 220/380 V, 3 kVA load. The experiment had consisted of open-loop test of known loads. The 3-phase loads were composed of 48 Ω resistance and 10 mH inductance for a balanced load. A future study will design software for the dsPIC microcontroller to generate all seven types of voltage sag

and to test the dynamic and nonlinear loads.

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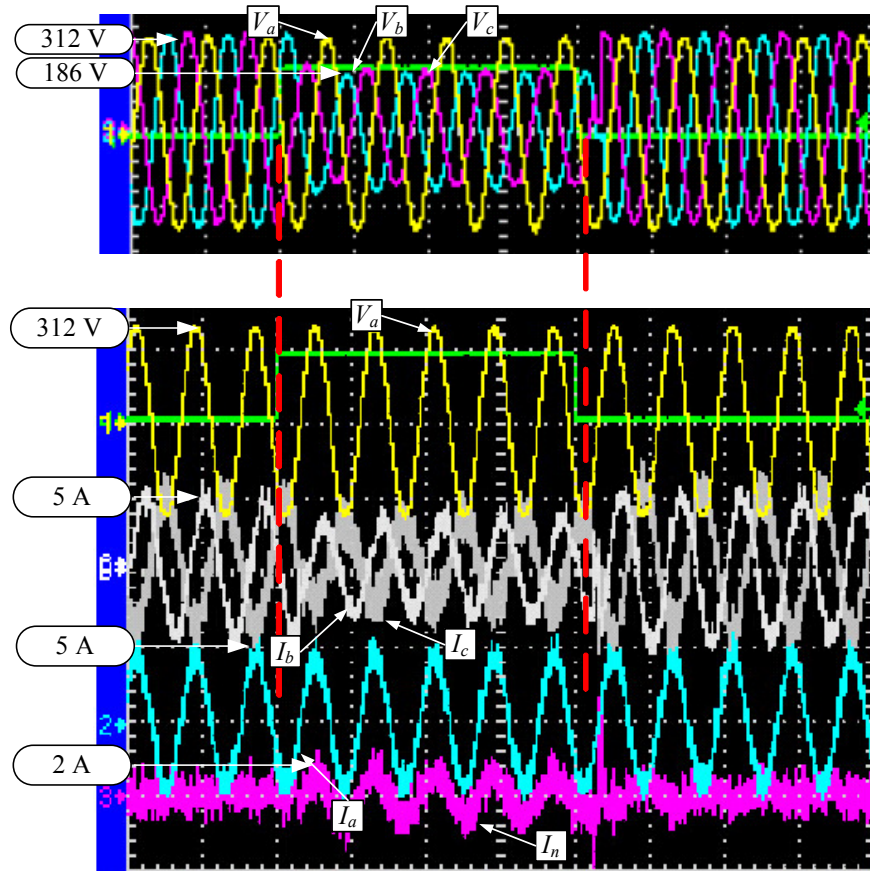


Figure 16. Voltage sag Type E.

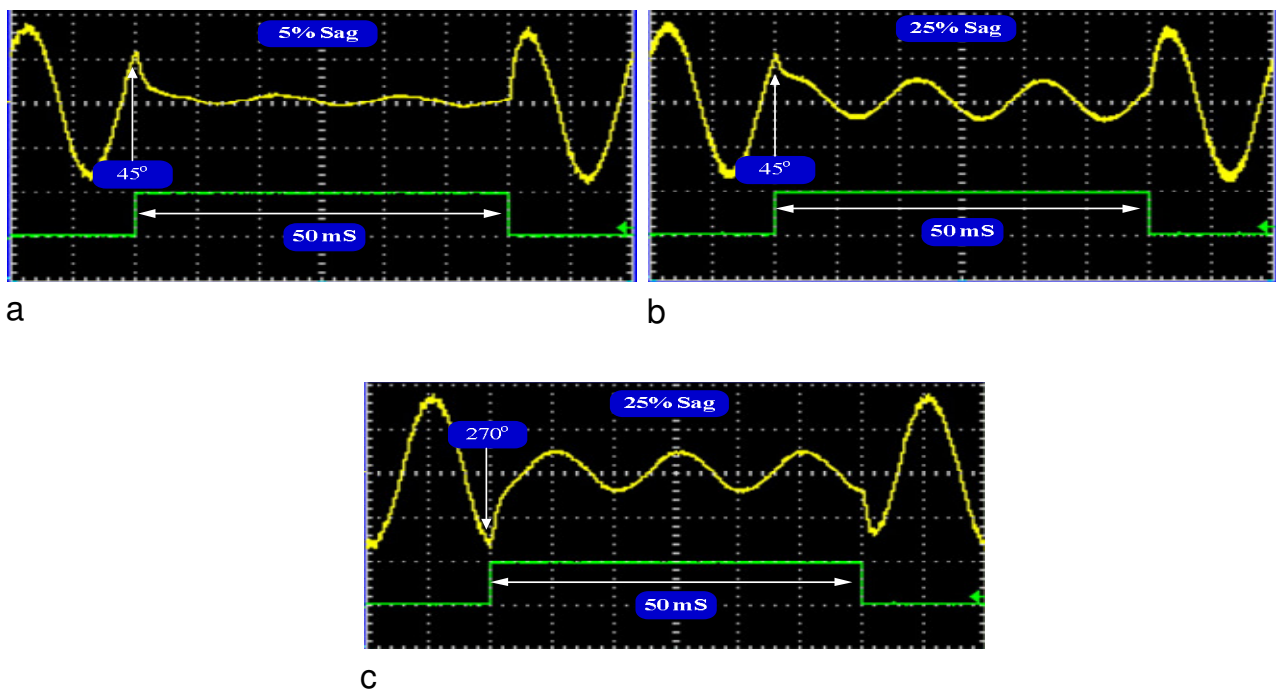


Figure 17. Experimental results: a, the point on wave at 45° with 5% sag; b, at 45° with 25% sag; c, at 270° with 25% sag.

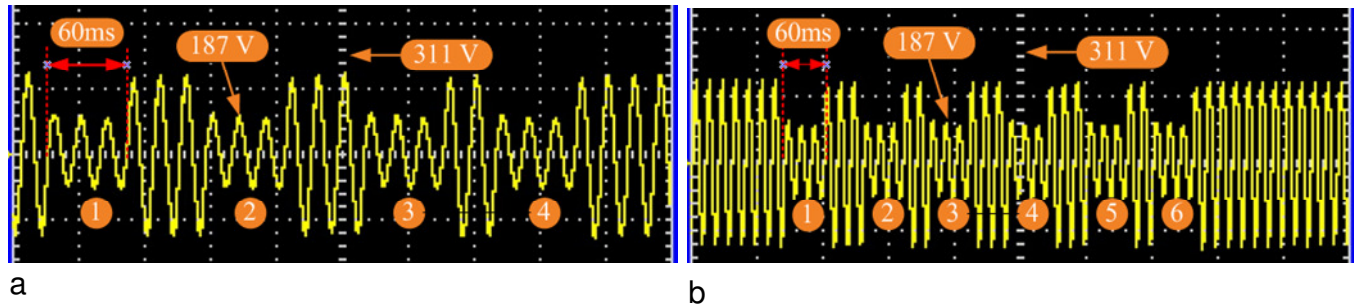


Figure 18. Experimental results: a, 4 repeated voltage sag; b, 6 repeated voltage sag

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REFERENCES

- Bollen MHJ (2000). Understanding Power quality problems voltage sags and interruption. New York, IEEE Press. pp. 193-196.
- Bhavsar S, Shah VA, Gupta V (2008). Voltage dips and short interruption immunity test generator as per IEC 61000-4-11. 15th National Power Systems Conference. Bombay, India.
- Collins ER, Morgan RL (1996). A Three-Phase Sag Generator for Testing Industrial Equipment. IEEE Transaction on Power Delivery. 11(1): 526-532.
- Ma Y, Karady GG (2008). A single-phase voltage sag generator for testing electrical equipments. Transmission and Distribution Conference and Exposition, Chicago IL, pp. 1-5.
- Oranpiroj K, Premrudeepreechacharn S, Kumsuwan Y, Boonsai T, Nayar CV (2005). A 3-Phase 4-Wire Voltage Sag Compensator Based on Three Dimensions Space Vector. Power Electronics and Drives System PEDS, pp. 1301-1305.
- Oranpiroj K, Premrudeepreechacharn S, Ngoudech M, Muangjai W, Yingkayun K, Boonsai T (2009). The 3-phase 4-wire voltage sag generator based on three dimensions space vector modulation in abc coordinates. International Symposium on Industrial Electronics ISIE2009, pp. 275-280.
- Oranpiroj K, Premrudeepreechacharn S, Ngoudech M, Muangjai W, Yingkayun K, Boonsai T (2009). The 3-phase 4-wire voltage sag generator based on abc algorithm. Electrical Engineering/Electronics, Computer, Telecommunications and Information Technology ECTI-CON 2009, pp. 82-85.
- Oranpiroj K, Premrudeepreechacharn S, Higuchi K (2010). SagWave for the 3-phase 4-wire voltage sag generator prototype. IEEE International conference on Control Applications CCA 2010, pp. 2209-2212.
- Perales MA, Parts MM, Portillo R., Mor JL, Leon JI, Franquelo LG (2003). Three-dimensional space vector modulation in abc coordinates for four-leg voltage source Converter. IEEE Power Electron., Lett., 1(4): 104-109.
- Perales MA, Prats MM, Portillo R, Mora JL, Leon JI, Franquelo LG (2004). Three-dimensional space vector modulation for four-leg inverters using natural coordinates. IEEE Inter. Symp. Ind. Electron. 2: 1129-1134.
- Rylande M, Grady WM, Arapostathis A (2007). Enhancement and application of a voltage sag station to test transient load response. IEEE Electric Ship Technology Symposium, Arlington VA. pp. 428-433.
- Takahashi R, Cortez JA, da Silva VF, Rezek AJJ (2008). A prototype implementation of a voltage sag generator. VIII Conferencia Internacional de Aplicacoes Industriais, Poços de Caldas, Brazil.
- Teke A, Meral ME, Tümay M (2008). Evaluation of available power quality disturbance generators for testing of power quality mitigation devices. Int. J. of Sciences and Techniques of Automatic Control and Computer Engineering, (special issue), pp. 624-635.
- Wu R, Chen D, Xie S (2005). A three-dimensional space vector modulation algorithm in a-b-c coordinate implemented by a FPGA. 31st Annual Conference of IEEE Industrial Electronics Society, (IECON 2005).
- Zhan C, Ramchandaramurthy VK, Arulampalam A, Fitzer C, Kromlidis S, Barnes M, Jenkins N (2001). Dynamic voltage restorer based on voltage-space-vector PWM control. IEEE Trans. Ind. Appl., 37(6): 1855-1863.
- Zhan C, Arulampalam A, Jenkins N (2003). Four-wire dynamic voltage restorer based on a three-dimensional voltage space vector PWM algorithm. IEEE Trans. Power Electron. 18(4): 1093-1102.