

Full Length Research Paper

New programmable BiCMOS fuzzifier

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It is clear that fuzzy logic is more compatible with analog circuit implementation compare to its digital mate. On the other hand being programmable is very important in various industrial implementations. Because of that this paper introduces a new method for implementing Membership function in fuzzy logic controllers. And a new high-speed analog fuzzification circuit was introduced for implementing this Idea and verified by Hspice simulations. It is characterized by a trapezoidal membership function with independently adjustable parameters. The core of the circuit is a BiCMOS current-mode circuit which works as a fuzzifier. The speed of controller is 20MFILIPS.

Key words: Fuzzifier, fuzzy controller, current-mode circuits, Mixed-Mode and BiCMOS.

INTRODUCTION

There are various circuit implementation methods CMOS, Bipolar and BiCMOS. In this paper we preferred BiCMOS implementation. BiCMOS is an evolved semiconductor technology that integrates two formerly separate semiconductor technologies - those of the bipolar junction transistor and the CMOS transistor - in a single integrated circuit device.

Bipolar junction transistors offer high speed, (Fuller et al., 2000; Min-Yuan Cheng et al., 2010; Rong-Jong Wai et al., 2002) high, and low output resistance, which are excellent properties for high-frequency analog amplifiers, whereas CMOS technology offers high input resistance and is excellent for constructing simple, low-power logic gates.

For as long as the two types of transistors have existed in production, designers of circuits utilizing discrete components have realized the advantages of integrating the two technologies (Meghraj Kachare et al., 2005); however, lacking implementation in integrated circuits, the application of this free-form design was restricted to fairly simple circuits. Discrete circuits of hundreds or thousands of transistors quickly expand to occupy hundreds or thousands of square centimeters of circuit board area, and for very high-speed circuits such as those used in modern digital computers, the distance between transistors (Mamdani et al., 1997; Hiroyuki

Watanabe et al., 1990) also makes the desired speeds grossly unattainable, so that if these designs cannot be built as integrated circuits, then they simply cannot be built.

Analog approaches are inherently faster and require much smaller silicon area and lower power consumption (Baturone et al., 1997, 1998; Nakamura et al., 2004). Their main disadvantage is that they are not so easily programmable. In this paper we present a new high-speed current-mod fuzzifier characterized by a trapezoidal membership function.

The fuzzifier presented in this paper suitable circuit to analyze and tune the nonlinear parameters of membership functions. These techniques provide a method for the fuzzy modeling procedure to learn information about a data set, in order to compute the membership function parameters that best allow the associated fuzzy inference system to track the given input/output data. This learning method works similarly to that of neural networks. Our discussions are started with summery of Nero-Fuzzy structures and back propagation algorithm and then describing BiCMOS structure along with circuit designs of fuzzifier.

In fact, because of that it is difficult to analyze highly nonlinear systems with classic methods, we convert classic world data into corresponding language terms.



Figure 1. Considering fuzzy as a new mapping space.

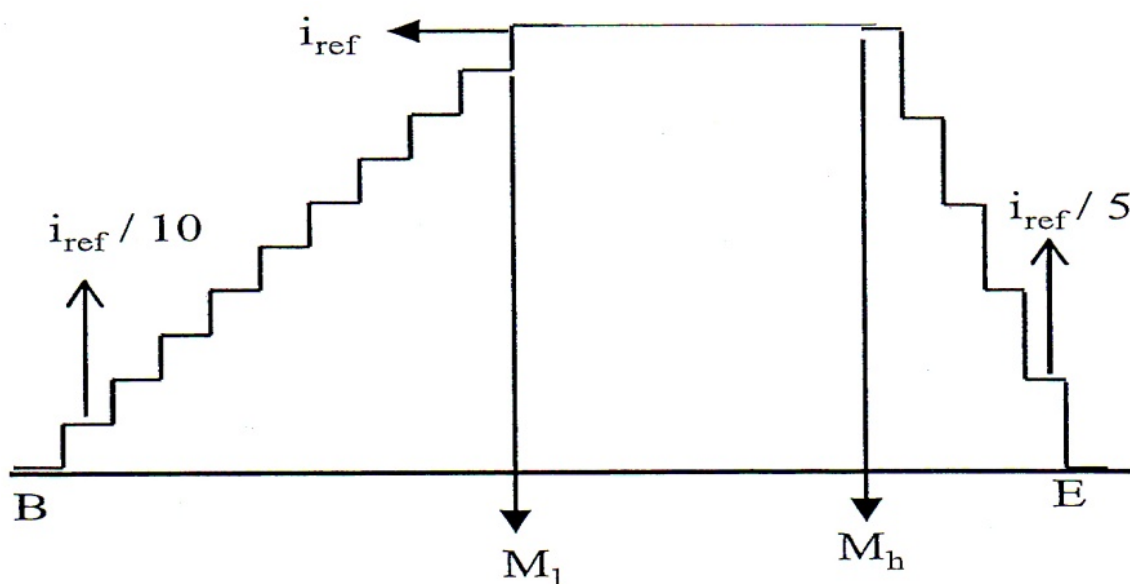


Figure 2. The shape of a trapezoidal membership functions with different slopes.

This application is said "fuzzifying" (Figure 1).

Therefore, for mapping classic world to fuzzy world, we need a circuit said Membership Function MFC. It is introduced a new design strategy for Fuzzifier implementation, in this paper. This method is the result of a new design method for digital fuzzy logic controller.

In this method all inputs and outputs of whole system are digital data, but the structure of different internal blocks is nearly analog.

Fuzzy membership definition

It is clear that general shape of a membership function which include triangle and ascending and descending ramps is as the nonsymmetrical trapezoidal shown in Figure 2, in which B is start point and E is the end, from B

to M_l and from M_h to E are ascending and descending slopes, respectively (Sadeq A, et al., 2011). The interval between M_l and M_h is plateau region which its value is corresponding to logical one.

In the strategy we introduced, input signal is digital and output membership degree is analog. As a result, we have considered horizontal axes as a digital data 5-bit (32 different binary states), but vertical axes as an analog signal in current-mode. It works in the range 58 A range.

The membership degree is as different and specific levels of current. Each level is a coefficient of a base current and this base current is specified according to the ascending and descending slopes.

The worst-case error is 1.3 μA , which is equal to 5-bit resolution. The circuit presented for fuzzifier is capable of performing different membership function shapes with deferent slopes.

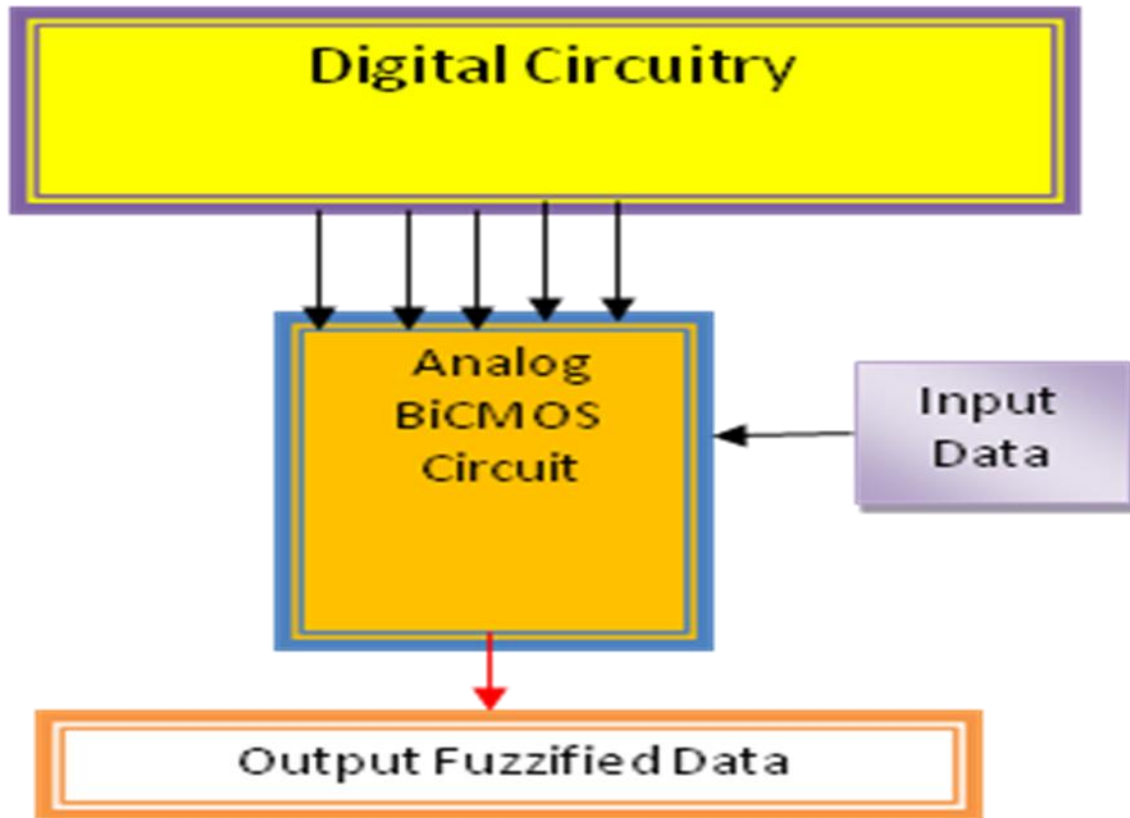


Figure 3. The relation between digital and analog part of Fuzzifier.

For example: if we chose $d_i = d_h$, $M_l < M_h$, it results a symmetric trapezoidal membership function.

Now, if we want to have descending slopes with lesser slope, we have to choose larger amplitude for d_l . There is an example in the Figure 2. If $E = M_1 = M_h$, $E = B + 6$ then $i_{base} = I_{ref}/5$ and the amplitude of levels are $i_{ref}/5$, $2i_{ref}/5$, $3i_{ref}/5$, $4i_{ref}/5$, $5i_{ref}/5 = I_{ref}$.

Changing E , we will have different descending slopes as described for some different values of B .

For ascending slopes, changing B with constant $M_1 = M_h = E$, we can similarly perform any arbitrary slope, for example if $E = M_1 = M_h$, $E = B + 11$ then $i_{base} = I_{ref}/10$ and the amplitude of levels are $i_{ref}/10$, $2i_{ref}/10$, $3i_{ref}/10$, $4i_{ref}/10$, $5i_{ref}/10$, $6i_{ref}/10$, $7i_{ref}/10$, $8i_{ref}/10$, $9i_{ref}/10$, $10i_{ref}/10 = I_{ref}$, as shown in Figure 2.

Considering examples mentioned above for performing ascending and descending slopes, choosing different values for parameters, we can have different triangular and trapezoidal shapes for performing membership functions, symmetrically or asymmetrically. There are some examples for clarification. Given $M_l = M_1$, $M_h = B + 9$, $E = M_h + 6$, we have a triangular membership function which its ascending slope has 10 steps with $i_{base} = I_{ref}/10$, that is, if input signal I becomes $B + 1$ the amplitude of output current will be $I_{ref}/10$, and if $I = B + 2$ then output

current becomes $2i_{ref}/10$, when $I = B + 10$ then output current will become reference current (I_{ref}). The descending slope of triangular has five steps while the step with I_{ref} amplitude is common between ascending and descending slopes. The base current in that case is one fifth of reference current. The output current in $M_1 = M_l$ is equal to reference current which is decreased $I_{ref}/5$ for everyone step respect to increasing input digital signal (I). That is, if $I = M_l + 1$ then output current is equal to $I_{ref} - I_{ref}/5 = 4i_{ref}/5$ and output current will be $i_{out} = 3i_{ref}/5$ as if $I = M_l + 2$. If $I = E$ then output current discusses to zero.

It was illustrated an unsymmetrical trapezoidal membership function in the Figure 2. The both side slopes of this membership function are the same as the triangular membership function mentioned above. But in this case we have different M_1 and M_h . The output current will remain reference current from M_1 to M_h .

The fuzzifier circuit algorithm

The main idea of the fuzzifier circuit is shown in Figure 3. Crisp input signal and the chosen parameters for performing favorable membership function, are applied to switch controller block and the output of this block are digital signals which control BiCMOS analog part.

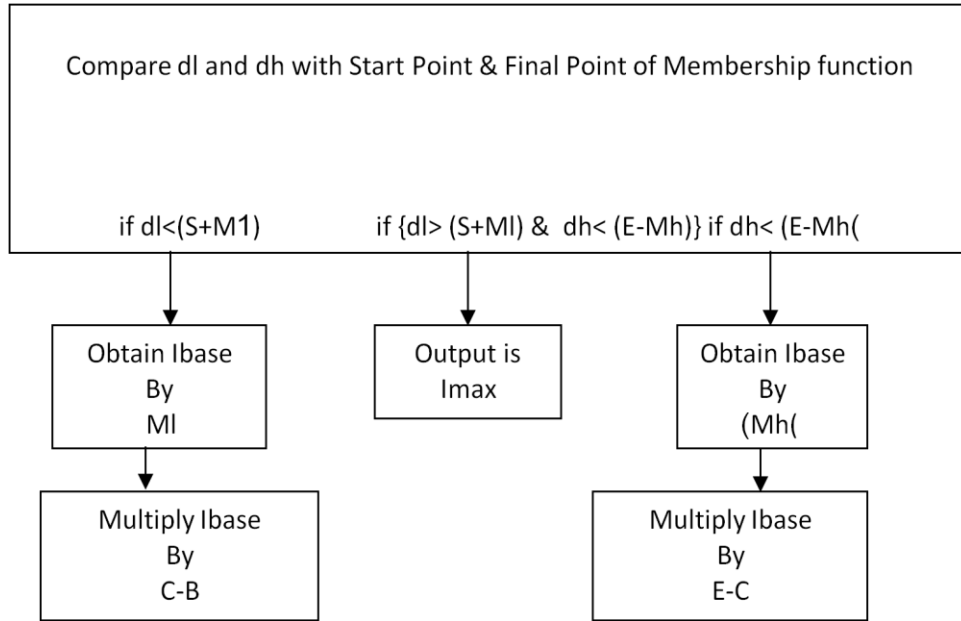


Figure 4. Block diagram of idea which fuzzifier has designed on it.

Input parameters are 5-bit numbers (B, M₁, M_h, E, d., dh) introduced in Figure 2. According to these parameters, the quotient is I_{base}. I_{base} will be multiplied by ordinal numbers between B and E.

If input signal is smaller than B or greater than E, the switches of right part of circuit will be disconnected and output current will be zero.

The more detailed way fuzzifier circuit works is illustrated in Figure 4. Considering the selection of parameters mentioned in Figure 2, all normalized membership functions only could take this values mentioned below for membership degree.

Fuzzifier circuit

Considering the descriptions mentioned before, and according to the B, Ml, Mh and E parameters, at first we have a division, which its numerator is reference current and its denominator is d₁ = M₁ - B or d₁ = E - M_h.

Figure 3 illustrates the different blocks of fuzzifier structure, and all blocks are illustrated in the Figure 5 in details. The dl and dh parameters at first entered to the carry generator part and considering previous description this action will be done with two separate parts, one for stimulate Linear voltage to current converter (LVCC) circuit. At last the obtained output of right current mirrors enters Gilbert translinear cells (GTC) which is discussed in detail (Jimenez et al., 1995).

The output current, I_{out}, is zero for negative input voltages V_d<0 (where V_d=V₁- V₂). It has a linear region

with constant slope s=I/R for 0<V_d<d_i and it saturates with a current I, for V_d>I.R. For V_d<0 the differential-pair current flows through transistor Match. This transistor works similar to a catch diode: it provides a path for negative currents to flow and prevents large voltage swings at the output node of the differential pair. This avoids degradation of the speed of the circuit this has a linear region in the range V_a<V_{in}<V_b. The left LVCC is used to set the bias (saturation) current of the right LVCC to a value I_{ba}=(V_b-V_a)/R. The output current of the right LVCC has the transconductance characteristic with a linear region in the range V_a<V_{in}<V_b, slope s=I/R and saturation current I_{ba}=(V_b-V_a)/R. A similar Arrangement is used to produce a Tran conductance Characteristic with a linear region V_{ic}<V_{an}<DVD and with saturation current (for V_{an}>DVD) I_{ed}= (V_d-V_c)/R. The all current sources shown in Figure 5 are equal and their size is 33 A.

All currents are equal and in linear regions in the ranges V_a<V_{in}<V_b and V_c<V_{in}<V_d respectively. The GTC is current multiplier/divider.

In Figure 5 for the left GTC I_i= (V_{in}-V_b)/R, I_l=(V_b-V_a)/R and I_o=I_{amp}. The output current is given by I_c=I_oI_{amp} (V_{in}-V_a)/(V_b-V_c). It has the piecewise linear characteristic shown on the left of Figure 5. Variables and parameters can be defined in the current domain according to, I_{amp}=V_{amp}/R, I_{in}=V_m/R, I_a=V_a/R, I_b=V_b/R, I_c=V_c/R and I_d=V_d/R. In this case the circuit of Figure 5 alone can be considered a current-mode fuzzifier. Currents I_{in}/ I_{amp}, I_a, and I_c can be replicated (and rectified) using current mirrors.

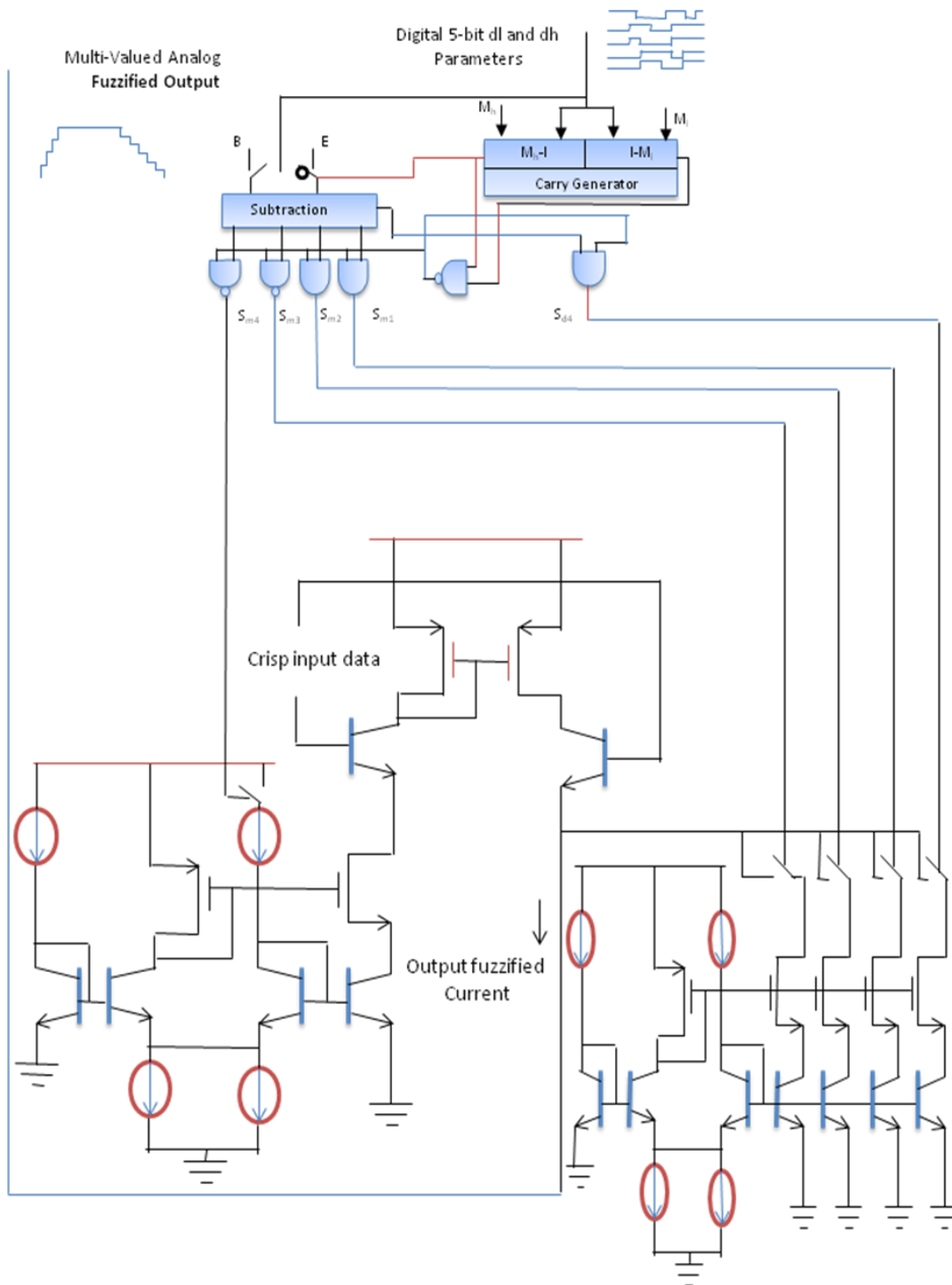


Figure 5. Proposed BiCMOS Fuzzifier.

Digital circuitry for switches controlling

The digital circuit illustrated below is used to control switches, shown in analog circuit in Figure 5. This structure was established of as-bit subtraction and two 5-

bit carry generator circuits and some extra logic gates and switches.

The dl and d, four-bit parameters are applied to this structure and will generate S_{d1} to S_{d3} for applying to LVCC circuit.

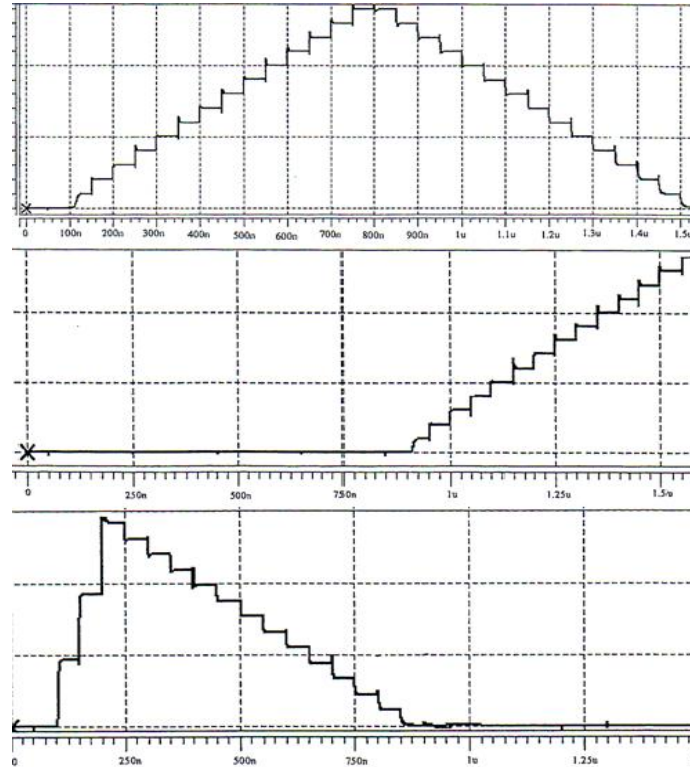


Figure 6. The obtained various MFCs.

Applying E, B and input signal (1) to this circuit yields S_{m1} , S_{m2} , S_{m3} , and S_{m4} for controlling GTC circuit.

S_{d4} and S_{d5} are produced to choose either Block 1 or Block 2, in order to specify the reference current is divided over one to fifteen.

RESULTS

HSPICE simulations using 2 µm BiCMOS technology N-well parameters (MOSIS) were performed. P and N transistors with dimensions 24/2 and 12/2 (in µm) were used for the simulations. Figure 6 shows the HSPICE simulated transfer characteristic of the fuzzifier circuit of Figure 5. The high speed rectifying characteristic can be verified with the transient response to a 1V, 10 MHz sine wave signal.

Figure 7 shows the trapezoidal DC transfer characteristic of the overall circuit for $V_a=0V$, $V_b=0.75 V$, $V_c=1.75 V$ and $V_d=3 V$. The systematic model of controller was evaluated using Anfis architecture training. To start training an FIS, first we need to have a training data set that contains desired input/output data pairs of the target system to be modeled. Sometimes we should have the optional testing data set that can check the generalization capability of the resulted FIS. Therefore the checking data set helps with model over fitting during

the training. The next stage is to specify initializing and generating of FIS parameters for Anfis training. In this paper we initialize the FIS with two inputs which one of them has three membership functions as shown in Figure 7a and the other one has three Trapezoidal shapes as shown in Figure 7b, nine rules and one output. After training, the improved and changed membership functions are obtained and shown in Figure 7. The total extracted control surface of controller is introduced and illustrated in Figure 8.

DISCUSSION

E. Alarcon (Alarcon et al., 1999) implemented a fuzzifier with a different strategy. They used the concept of the implicit signal-to-time conversion in the PWM process. M. Azeem (Mohammad Fazel Azimi et al., 2006) proposed a fuzzifier for Sugeno-Takagai's fuzzy logic controller. They used normal current-mode dividers.

The analog implementation of a generalized fuzzification scheme was introduced in (Sanchez et al., 2002).

The work which has done in this paper compare to works mentioned above has better functionality and compatibility. High speed operation was also verified with simulations. The scheme uses circuits which can operate

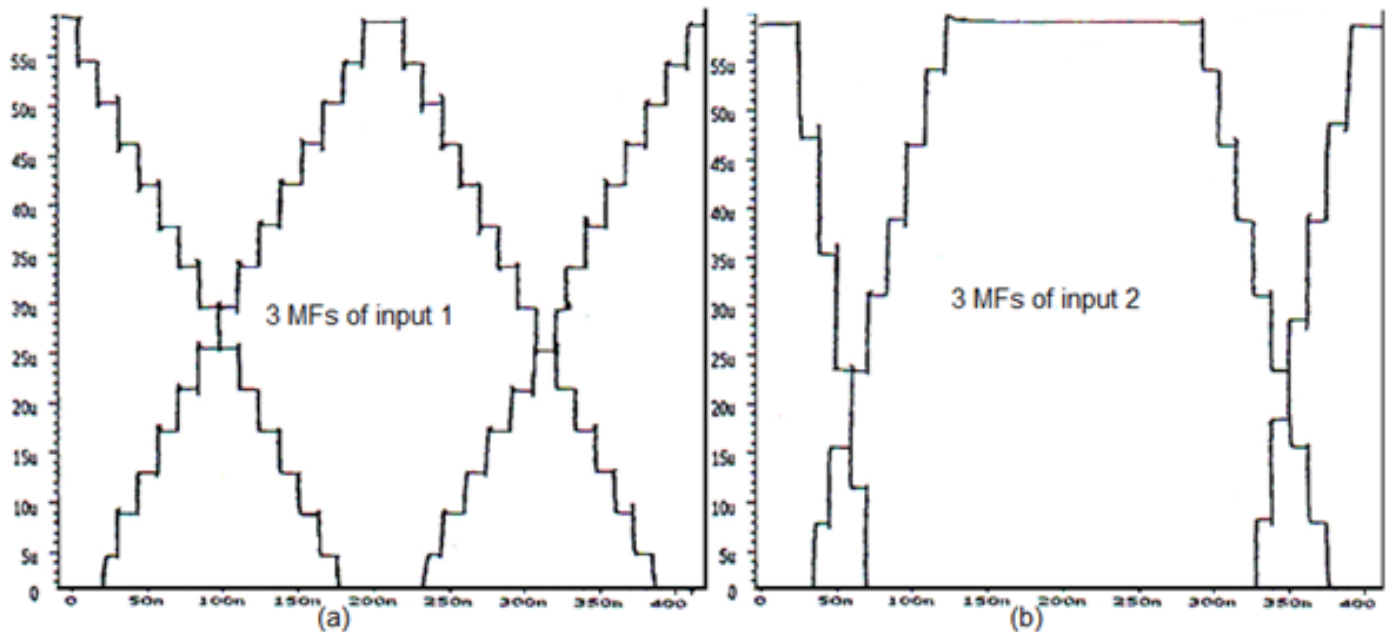


Figure 7. Hspice simulations output of proposed fuzzifier which produces all types of membership functions applicable to a two-input one-output controller.

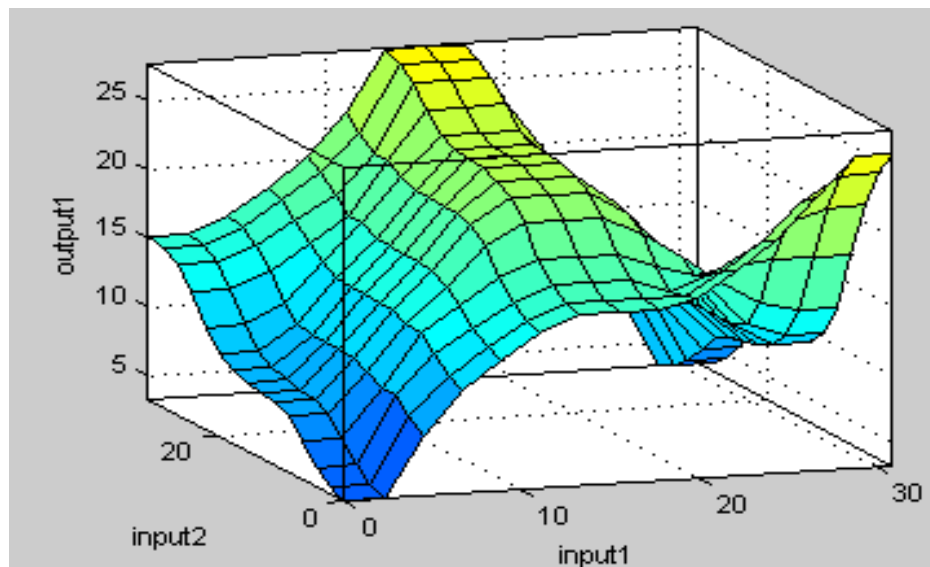


Figure 8. The obtained control surface of proposed controller.

with low supply voltages (single 3.3 V supply) and requires very compact circuitry (less than 30 transistors). It can find utilization in applications where high adaptable fuzzifiers with constant singleton coefficients are required. The main drawback of this work is the problem of fabrication due to using both NPN and PNP bipolar transistor types with CMOS transistors.

Conclusion

This paper introduces a new method for implementing Membership functions in fuzzy systems. And a new high-speed analog fuzzification circuit was introduced for implementing this Idea and verified by simulations. It is characterized by a trapezoidal membership function with

independently adjustable parameters. The core of the circuit is a BiCMOS current-mode circuit which works as a fuzzifier. This scheme is expected to find application in neuro-fuzzy processors where adaptation of the membership function parameters is required. The result is a faster, cheaper and higher controllable compare to conventional fuzzification techniques This fuzzifier has applied to a two input one output controller and has shown good results.

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