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Full Length Research Paper

Field-programmable gate array (FPGA)-based designed using VHDL hardware description language transmission performance analysis of binary phase shift keying (BPSK) and quadrature phase shift Keying (QPSK) modulators

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Binary phase shift keying (BPSK) and quadrature phase shift Keying (QPSK) modulation techniques are often proposed for satellite communications and band-limited communication channels; however, both modulations are important in high speed data communications. High speed data communications are implemented on high speed hardware in wireless systems. The paper presents the design of a QPSK and BPSK digital communication modulators and their implementations on high speed field-programmable gate array (FPGA) using Quartus II. Also, for these modulation schemes, resource utilization was introduced. Both modulations were designed in Quartus II using VHDL hardware description language. It was shown that transmission of QPSK modulator is fast than transmission of BPSK modulator at the same bit error performance. According to BPSK, QPSK modulator uses more memory. But other resources equal to for these modulation. Principles of the BPSK modulation and QPSK modulation are illustrated using schematic diagrams. The analysis of theoretical aspects of the BPSK and QPSK modulations are represented. Both modulations waveforms are illustrated using a simulation program. Implementations of the BPSK and QPSK systems on FPGA are shown using algorithms of modulator.

Key words: Binary phase shift keying (BPSK), quadrature phase shift Keying (QPSK), field-programmable gate array (FPGA)

INTRODUCTION

In recent years, with the high-speed development, satellite communication has been implemented in various areas, such as remote sensing, mobile communication, digital satellite TV and so on (Tianjun and Wenrui, 2008). In satellite communication systems and navigations systems, the Binary phase shift keying (BPSK) and quadrature phase shift Keying (QPSK) modulation techniques are very popular. At present, BPSK modulation is used for telecommand and telemetry system while QPSK is for payload data transfer (Sharma et al., 2010). Both BPSK and QPSK modulations are based on phase modulation.

Design of field-programmable gate array (FPGA) based QPSK and BPSK modulators were presented previously. In a realized work, performance comparison of QPSK and BPSK were presented. However, in this work such as resource utilization or power consumption, device utilization was not introduced (Popescu and Gontean,

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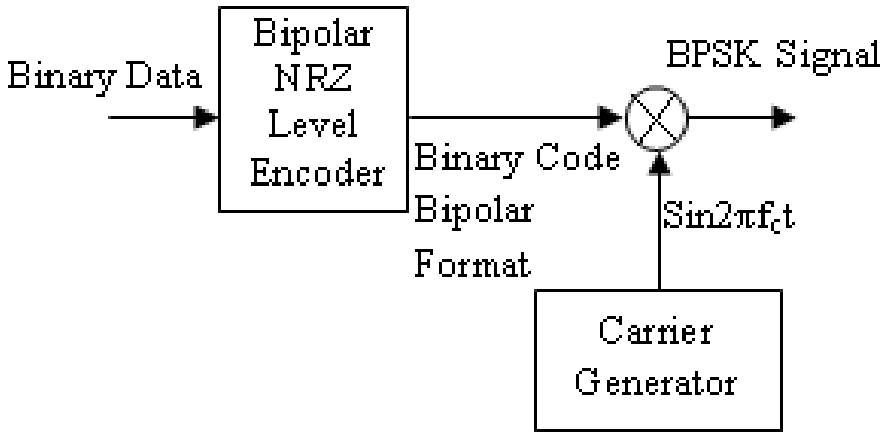

Figure 1. Principle of BPSK modulator.

2011).

A QPSK modem was created using FPGA. In this paper, modulator and demodulator is embedded on same FPGA kit. In the design, direct digital synthesis principle was presented. In this paper, simulation results of output wave were only introduced (Song and Yao, 2010). In the other work, QPSK modulator was presented. In this paper, resource utilization in device was only presented. However, all the information obtained were about power consumption (Popescu et al., 2011). Data rate of a designed FPGA based QPSK modulator is about 2 Mbps. In this design, for carrier signal, using square wave signal QPSK modulator was created (Elamary et al., 2009).

This paper mainly concentrates on the hardware realization of modulators for BPSK and QPSK techniques. These modulator schemes were created by the fastest data transfer method. In the design, each sample of output signal is obtained approximately, each clock time using mux-based algorithm. One of the most important issues is power consumption and resource utilization on FPGA device. Although, in numerous studies, FPGA-based QPSK modulator or BPSK modulator was presented, resource utilization or power consumption issues were not discussed. In order to reveal these unclear issues, such as resource utilization and power consumption, device utilization was also presented in this work. Comparison of resource utilization and power consumption was realized and the simulation results were presented. Additionally, the design of this study was compared to those of previous works.

BPSK MODULATOR AND DEMODULATOR

BPSK modulation can be considered for two cases: 0 and 1. BPSK modulated signal is change at this cases. Data bits are multiplied with a carrier signal and then modulated signal is created. Figure 1 shows a principle BPSK modulator.

Carrier signal is generated by carrier generator and it is multiplied with data bits, so BPSK signal is created. If transmitting data bit is 1, generated carrier signal is not shifted. But if transmitting data bit is 0, phase of carrier sinusoidal signal changes by 180° (Das, 2010). Figure 2 shows BPSK modulation. In this figure, m(t) is message signal, c(t) is carrier signal and s(t) is modulated signal.

In BPSK, the transmitted signal is $s(t) = m(t)c(t)$ and scheme of BPSK modulation is as follows (Das, 2010) and f_c is the frequency of the carrier,

$$s(t) = A_c Cos(2\pi f_c t) \text{ if m(t)= logic 1}$$

$$s(t) = -A_c Cos(2\pi f_c t) \text{ if m(t)= logic 0} \quad (1)$$

In BPSK demodulator, binary baseband data can be achieved from the BPSK waveform by using coherent detector. As shown Figure 3, the modulator consists of a multiplier, an integrator and a decision device. The incoming BPSK signal is firstly multiplied with a carrier of same phase and frequency to that of the carrier used in the transmitter section. Next, output signal of multiplier is passed through integrator, then integrated signal is passed through a decision making device (Das, 2010).

In Figure 3, output of integrator is compared to threshold. If output of integrator is higher than threshold, output of comparator is marked symbol 1 by comparator; otherwise output of comparator is symbol 0.

QPSK MODULATOR AND DEMODULATOR

Among all M-ary PSK schemes, the QPSK (Quadrature Phase Shift Keying) is the most often used and the bandwidth efficiency is increased (Xiong, 2000). The signals of the QPSK modulation are defined in (3),

$$S_{QPSK}(t) = A_c \cos(W_c t + \phi_i) \text{ for i=0,1,2,3} \quad (2)$$

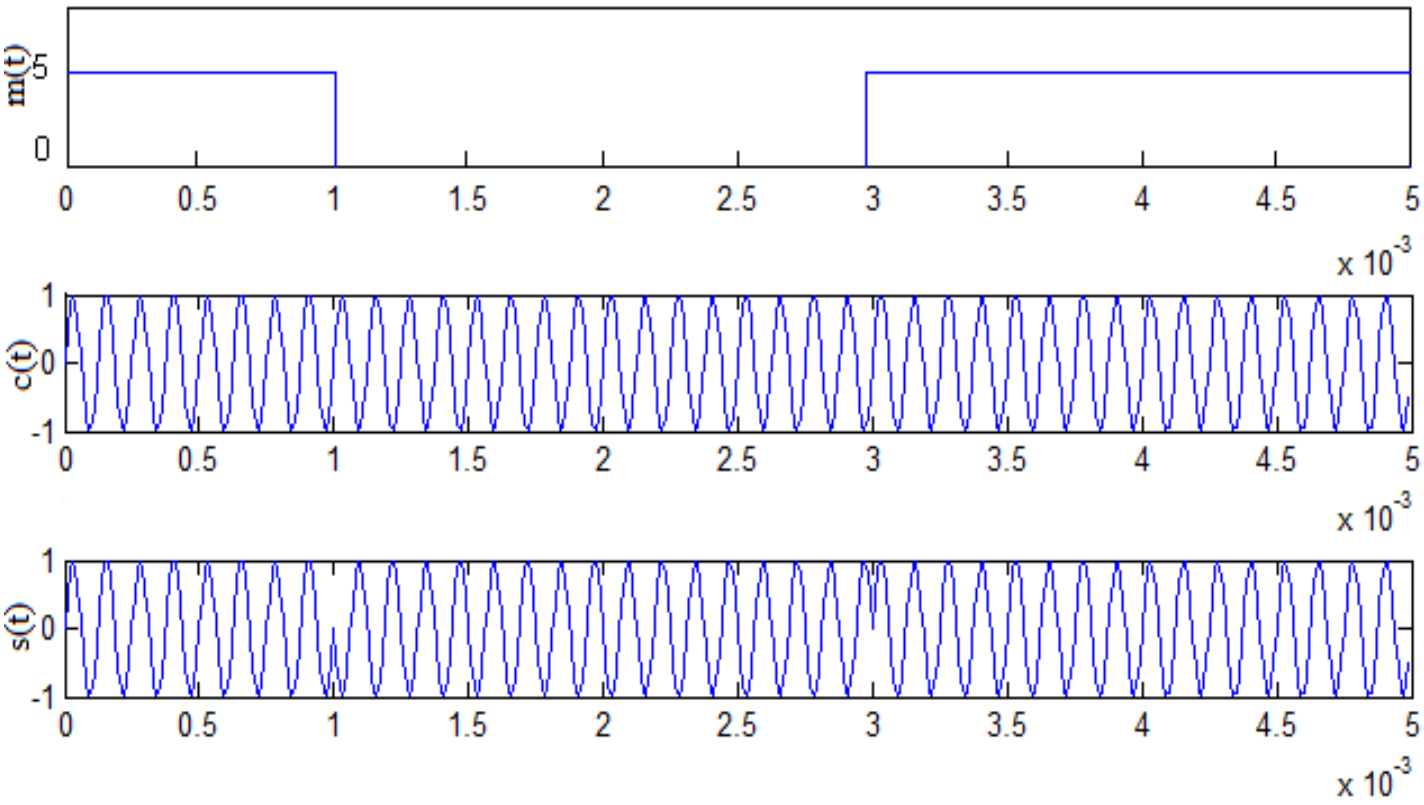

Figure 2. BPSK modulation.

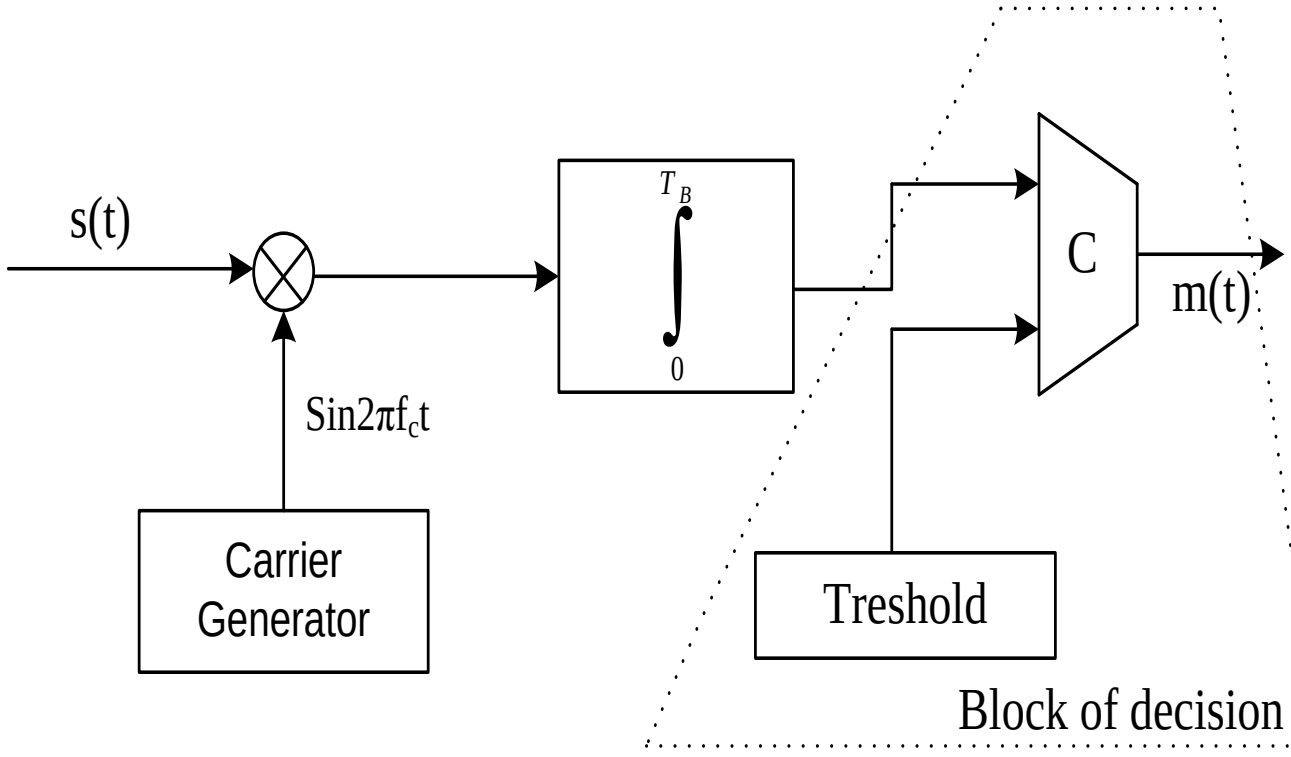

Figure 3. Principle of BPSK demodulator.

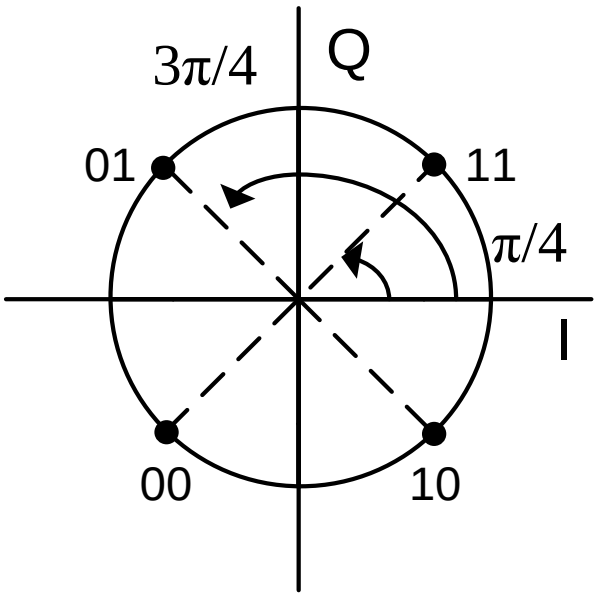

Figure 4. I-Q diagram of QPSK modulation.

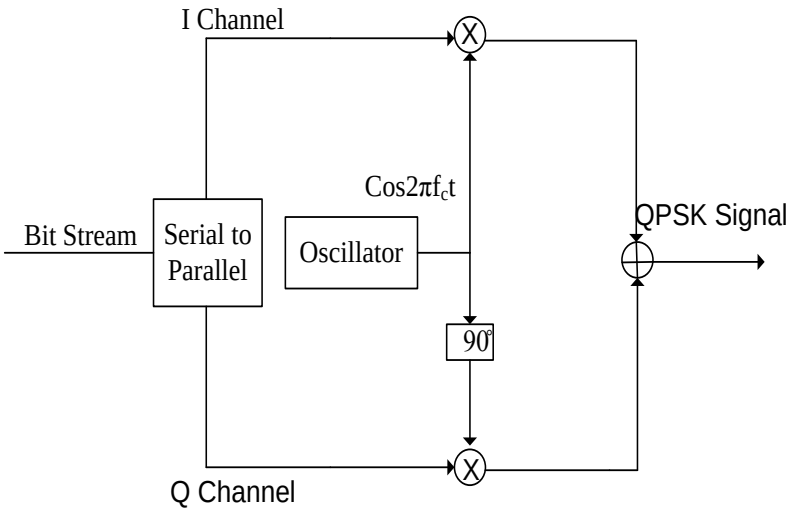

Figure 5. Principle of QPSK modulator.

In Equation (2), $\Phi_i=(2i+1)*(\pi/4)$. For i=0, $A_c=1$;

$$S_{QPSK}(t) = A_c \cos(W_c t + \pi/4)$$

$$= \frac{1}{\sqrt{2}}(\cos W_c t - \sin W_c t) \quad (3)$$

Thereby, BPSK modulation can be considered for four cases: 00, 01, 10 and 11. These cases are shown in Figures 4 and 5.

The binary sequence is separated by the serial-to-parallel converter and just as odd bit sequence pass through I channel, even bit sequence pass through Q channel. Figure 6 shows QPSK modulation. In this figure, *$m_1(t)$* and *$m_2(t)$* are message signal, *Q-ch* and *I-ch* are Q channel and I channel signals respectively, *s(t)* is modulated signal.

VHDL AND QUARTUS II

The very high speed integrated circuit Hardware Description

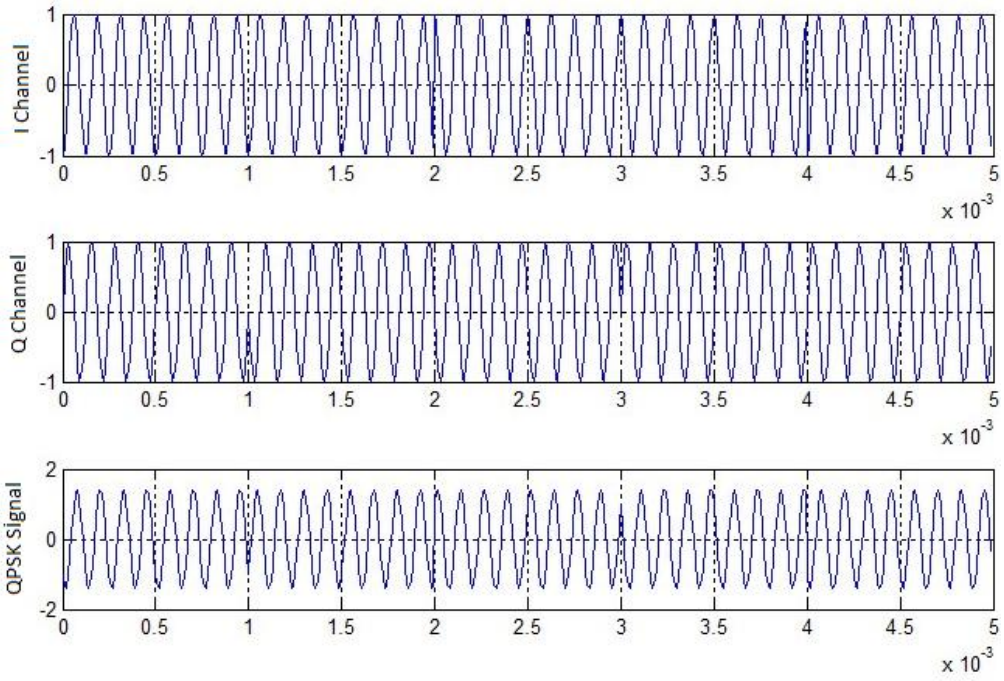

Figure 6. QPSK modulation.

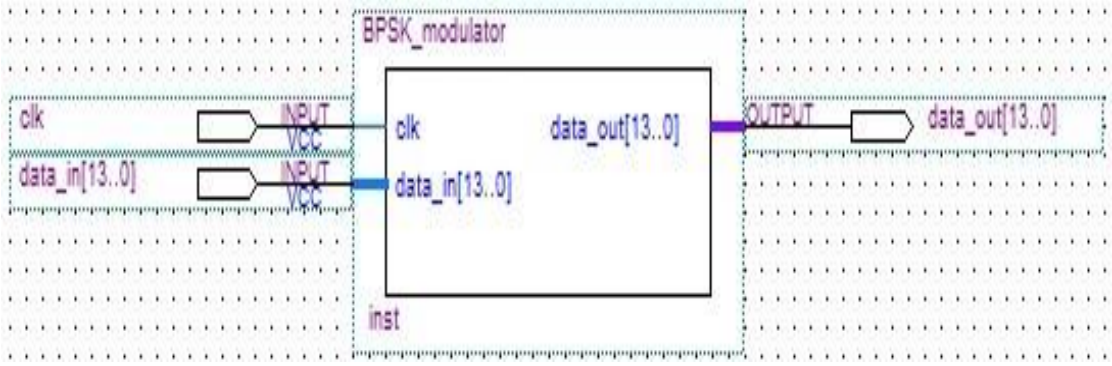

Figure 7. In Quartus II created BPSK block

Language (VHDL) text files (with the extension.vhd) were created with the Quartus II. These files consist of control block, mux, rom, bit separator and counter. Then, created blocks are synthesized and validated. If validation is successful, simulation files can be created. Simulation files was already created and saved in the same folder, all with the extension sim.

BPSK MODULATOR BASED ON FPGA

BPSK modulator was implemented on the *Cyclon III* kit board. Board was used both modulator and demodulator. Thereby used board was behaved as a modem. In this paper, the modulator was represented. The principle of the BPSK system implemented on the FPGA is shown in Figure 6.

In Figure 6, message signal is sampled, quantized and coded by ADC. BPSK modulation modulates bits one by one. So that, bit separator was used in this paper. Bit separator was created using very high speed integrated circuit Hardware Description Language.

According to output digital signal of bit separator (0 or 1), mux selects one of sin or delayed sin. So, BPSK modulated signal was created. In Quartus II, created block of BPSK modulator is shown in Figure 7.

In Figure 7, *clk* is clock pulse, *data_in* is input of ADC and *data_out* is BPSK modulated signal. *BPSK_modulator* block contains 5 blocks, namely, control block, rom, counter, bit separator and mux. Here, the

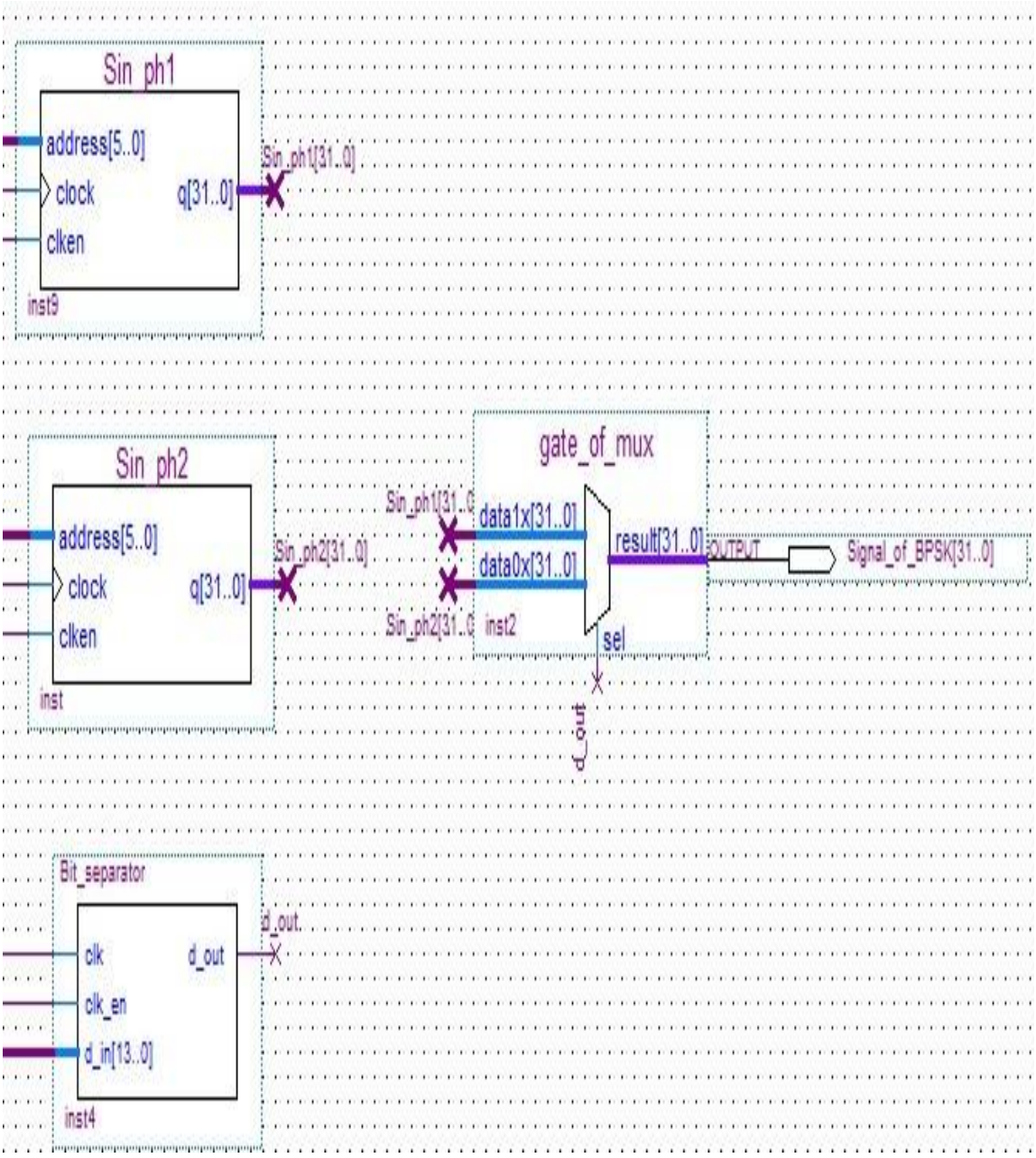

Figure 8. BPSK modulator in Quartus II.

control block controls all the operations of the transmitter and the timing for the transmitted bits, enabling the counter, bit separator and rom.

In Figure 8, Sinus data's was saved on *sin_ph1* and *sin_ph2. sin_ph2* is delayed by 180°. Also, *d_out* is output of bit separator. *Gate_of_mux* acts as a selector.

QPSK MODULATOR BASED ON FPGA

QPSK based on FPGA application was implemented on Quartus II compiler. Also, both modulation and demodulation were implemented on FPGA. So, modem based on FPGA was created. Yet, in this paper QPSK modulator was only represented using Quartus II complier. The principle of the QPSK system implemented on the FPGA is shown in Figure 9.

The output of created bit separator using very high speed integrated circuit Hardware Description Language has two bits. According to output digital signal of bit separator (00, 01, 10, 11), mux selects one of four cases. Thereby, QPSK modulation was created on FPGA.

In Figure 10, clk is clock pulse, data_in is input of ADC and data_out is QPSK modulated signal. Also, this

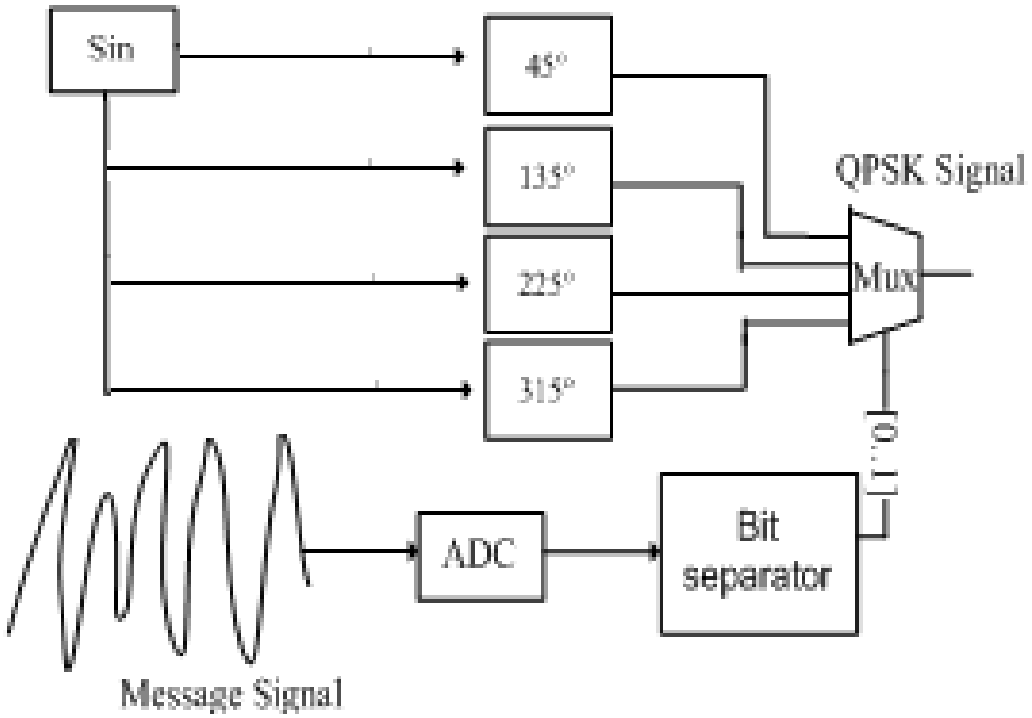

Figure 9. Principle of the QPSK system implemented on the FPGA.

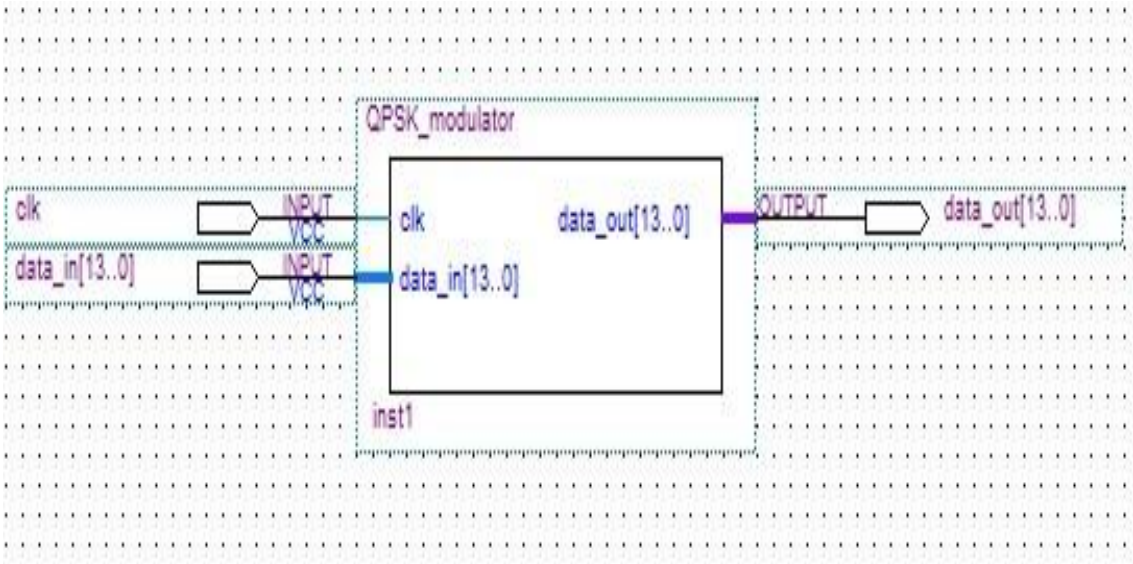

Figure 10. In Quartus II created QPSK block.

modulator contains four counters and roms, control block, bit separator and mux. In Figure 11, it is shown that blocks of implemented QPSK modulator in FPGA. According to output of bit separator, one of *ph1, ph2, ph3* or *ph4* is selected by *gate_of_mux*. Using control block, other blocks are controlled during operating time. The output of control block is enabling signal. So, to enable operating block this block is used. Figure 12 shows the control block.

QPSK AND BPSK BER

In an AWGN channel, the bit error rate (BER) decreases

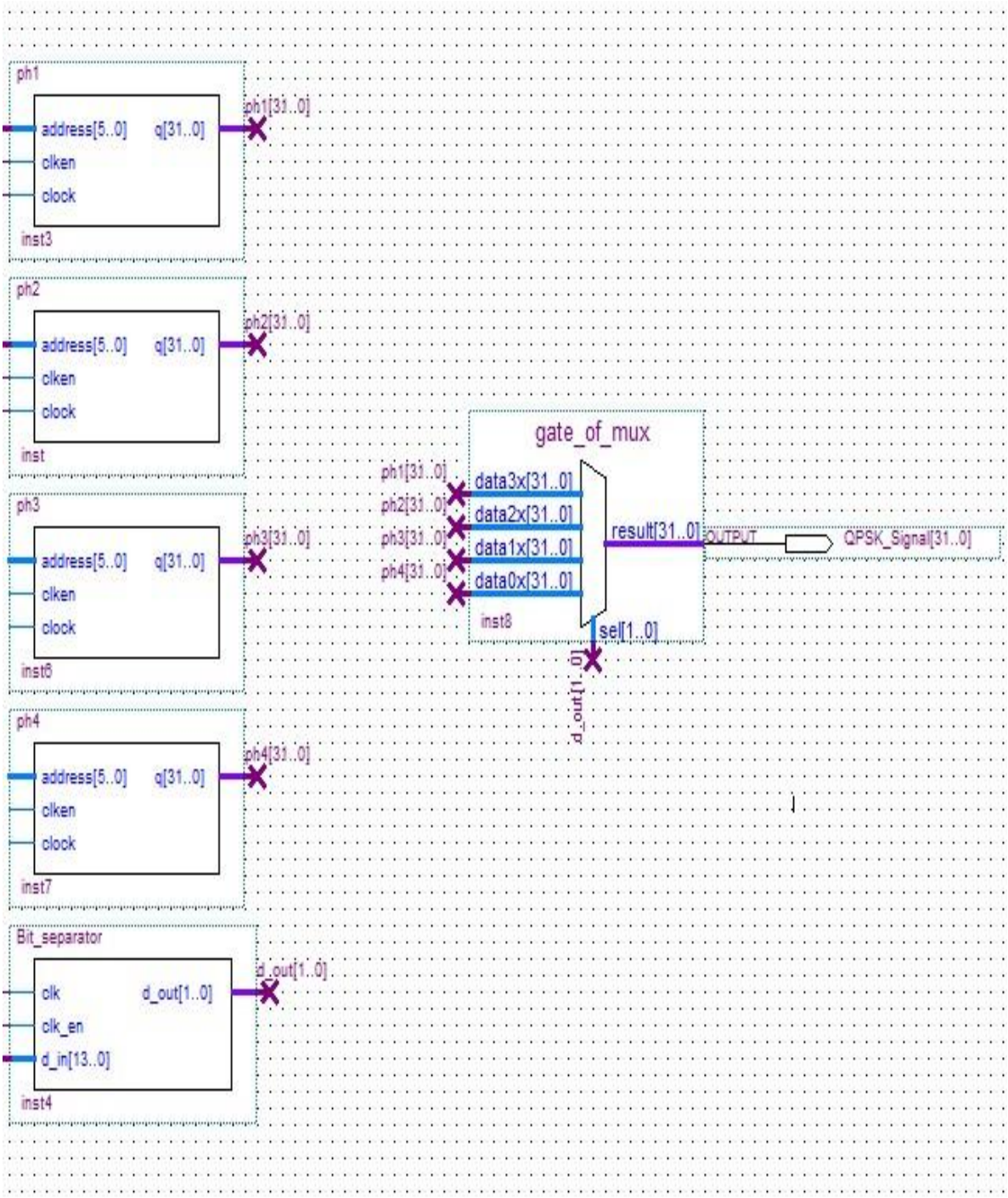

Figure 11. QPSK modulator in Quartus II complier.

approximately exponentially as the signal to noise ratio (SNR) increases (Xiong, 2000).

Straight BPSK and QPSK produce good BER value at the receiver. Although the symbol error rate for BPSK is twice that of QPSK, QPSK transmits symbols at only half the rate of BPSK when both are sending data at the same bit rate, so their BER performances are equivalent (Morrow, 2004). Bit error rate can be shown at Equation 4.

$$P_b = Q\left(\sqrt{\frac{2E_b}{N_0}}\right) \quad (4)$$

In Equation (4), E_b and N_0 represents average energy per

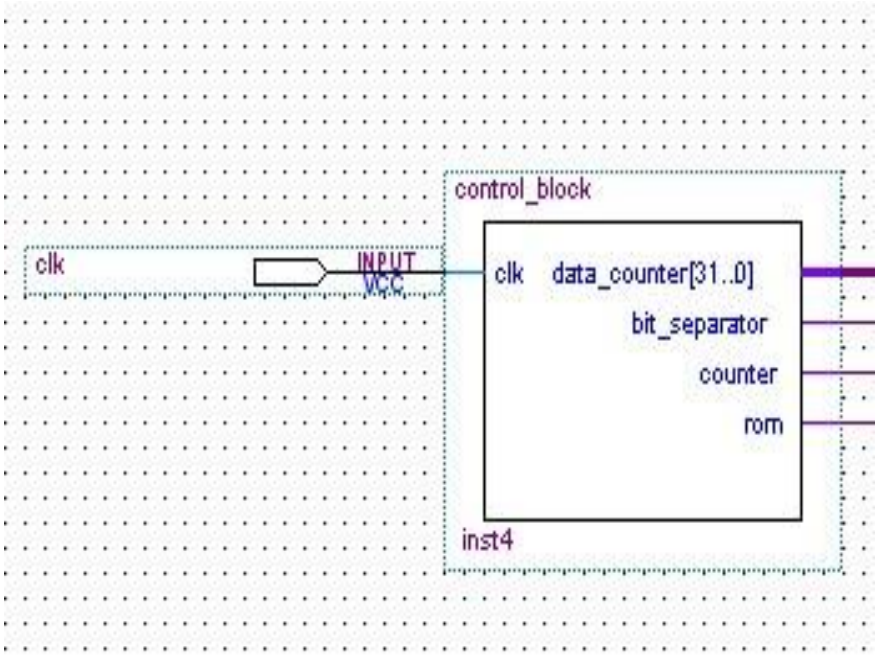

Figure 12. For QPSK modulator control block.

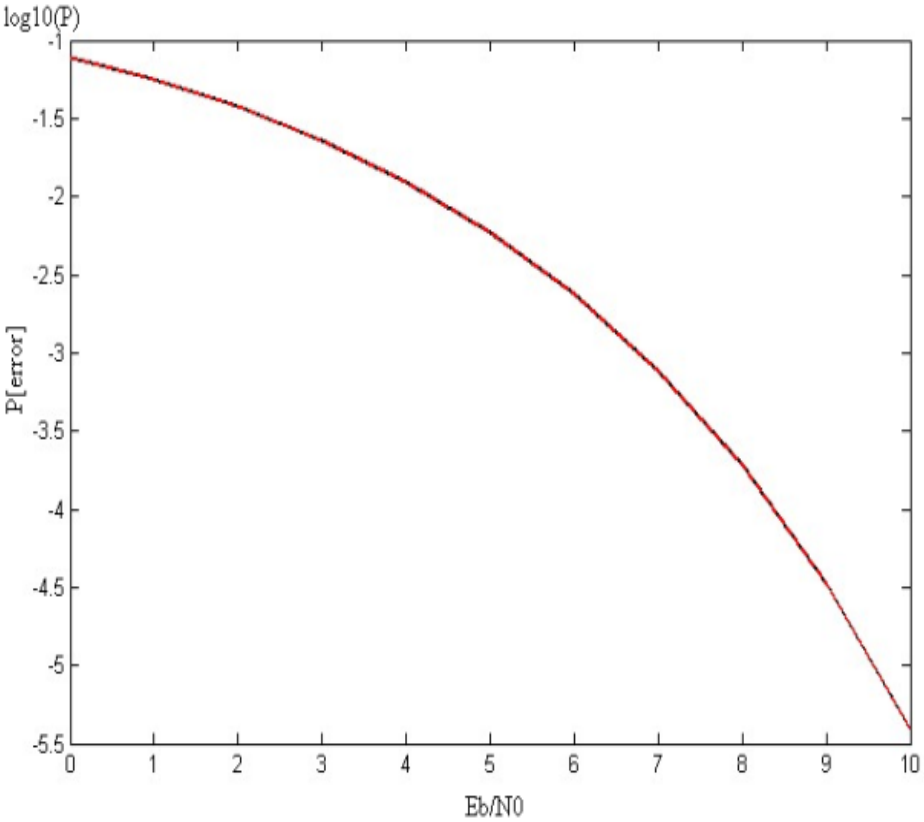

Figure 13. BER of QPSK and BPSK modulation techniques.

bit and noise power, respectively. Figure 13 shows BER performance of BPSK and QPSK modulation.

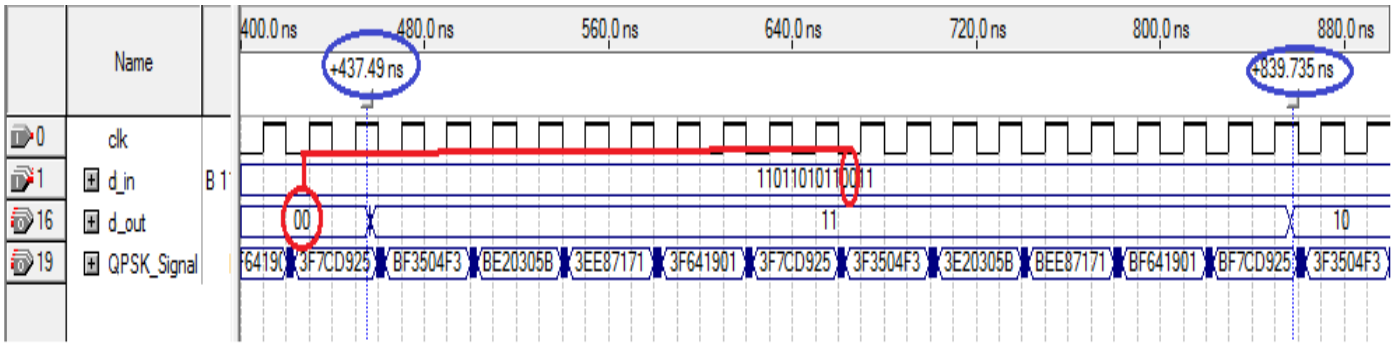

Figure 14. Simulation result of QPSK.

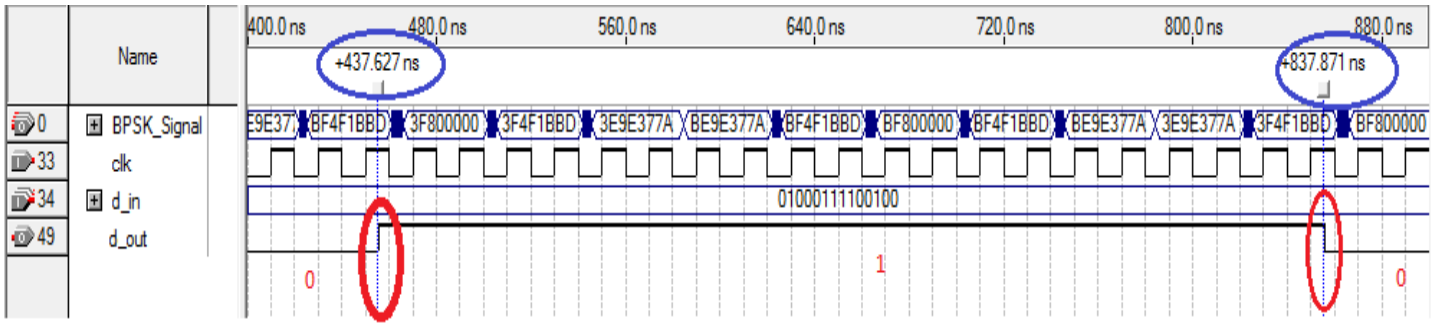

Figure 15. Simulation result of BPSK.

QPSK AND BPSK MODULATİON BASED ON FPGA

The waveform obtained with the QPSK simulation is presented in Figure 14 and simulation results with the BPSK are introduced in Figure 15. As shown Figure 14 and Figure 15, while two symbols is transmitted on 400 ns using QPSK modulation, one symbol is transmitted on 400 ns using BPSK modulation.

d_in is output of ADC, namely, input of bit separator. Each sample of *QPSK_signal* was signified 32 bit. Also, each sample was shown using hexadecimal numbers. This numbers can be converted decimal form using Matlab. The hexadecimal numbers represent the samples of QPSK signal, namely, if this digital numbers are plotted in Matlab or plotting programs, QPSK modulated signal is obtained (Figure 6). *d_out* is output of bit separator. As shown Figure 14, dual bits are produced using *d_in*. As dual bits cases, transmitting signal changes.

CONCLUSIONS

This paper is aimed at performance comparison of BPSK and QPSK modulator. This comparison consists of modulating time, power consumption and resource utilization. Also, this work is compared to previously works. Some of these papers only concentrated on modulator design, others both modulator designs created and power consumption and resource utilization concentrated.

As shown in Figure 14, one symbol is transmitted on about 400 ns (837 to 437 ns) for QPSK. For BPSK, this value is obtained at time of one bit modulating. At this case, data transfer rate of QPSK is 5 Mbps. In some papers, this value is 10 Kbps and 2 Mbps, respectively (Popescu et al., 2011; Elamary et al., 2009) but this algorithm (mux-based design) do not implemented on multiplexing systems (such as OFDM, CDMA) and clock signal is selected 50 MHz. If any multiplexing technique is used with higher clock signal, data transfer rate will increase to about 100 to 200 Mbps.

Figures 16 and 17 show resource utilization for BPSK and QPSK modulator. While total memory bits are 1280 for QPSK, this value is 640 for BPSK modulator. The reason for this difference, QPSK modulator uses two times ROM according to BPSK modulator. Also, I/O pins are same for these modulators. If floating point numbers are fixed point numbers, I/O pins will be about 25. Because floating point numbers are obtained using 32 bits in this paper. Also, input pin number is selected to considering 14 bits ADC. For proposed QPSK modulator algorithm, I/O pin number is 50 in (11). So the used signal frequency or phase is not required to change, as such, PLL was not used in this work.

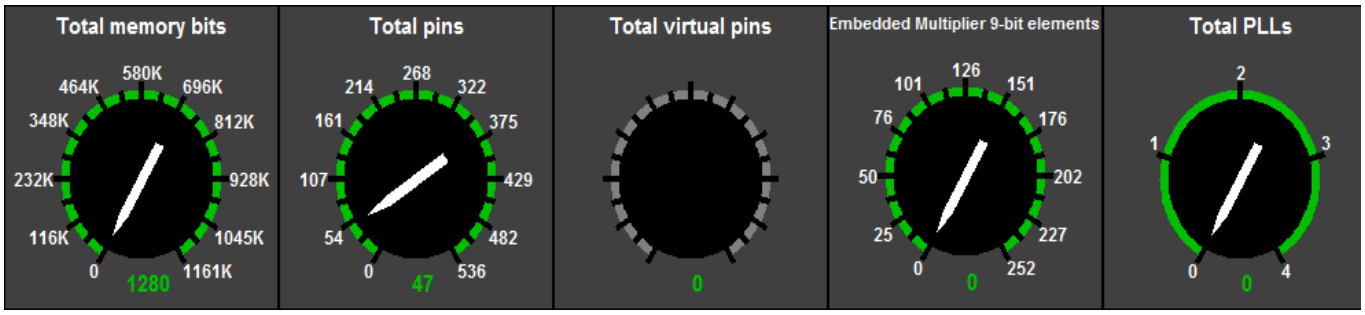

Figure 16. Resource utilization of QPSK.

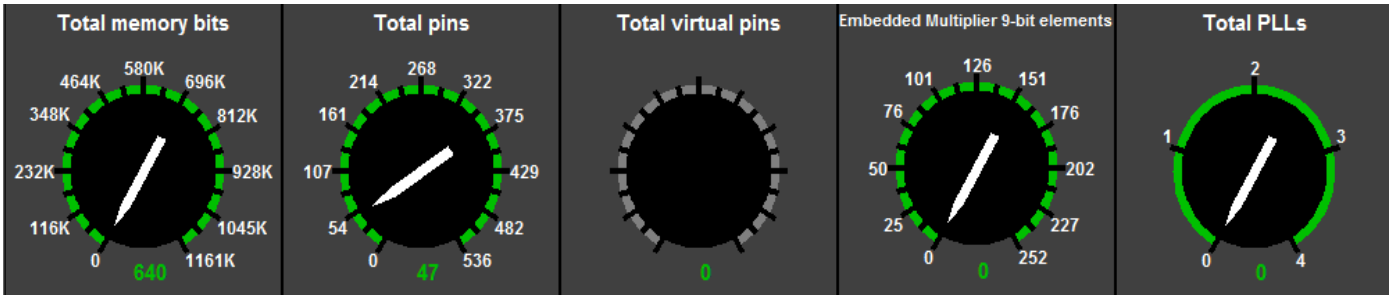

Figure 17. Resource utilization of BPSK.

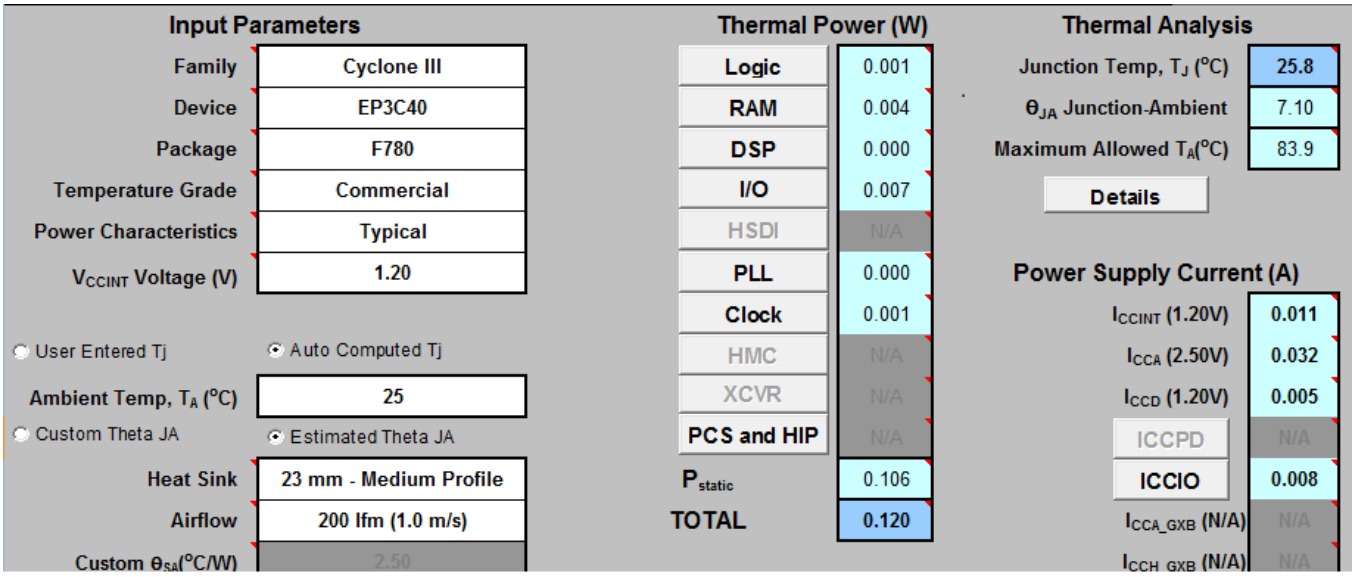

Figure 18. Estimating power of QPSK.

For the 50 MHz clock signal, the power consumption obtained with the QPSK and BPSK modulators is presented in Figures 18 and 19. As shown in these figures, QPSK modulator consumes 14 mW while BPSK modulator is 12 mW out of P_{static}. Really, as introduced in Figures 18 and 19, power consumption is very much affected by the I/O pin number. In (11), for proposed QPSK algorithm, power consumption is 28 and 19 mW.

As shown in simulation results, QPSK modulator is work efficiently according to BPSK. According to both BER result and data rate transfer, power consumption and resource utilization results, QPSK modulator has

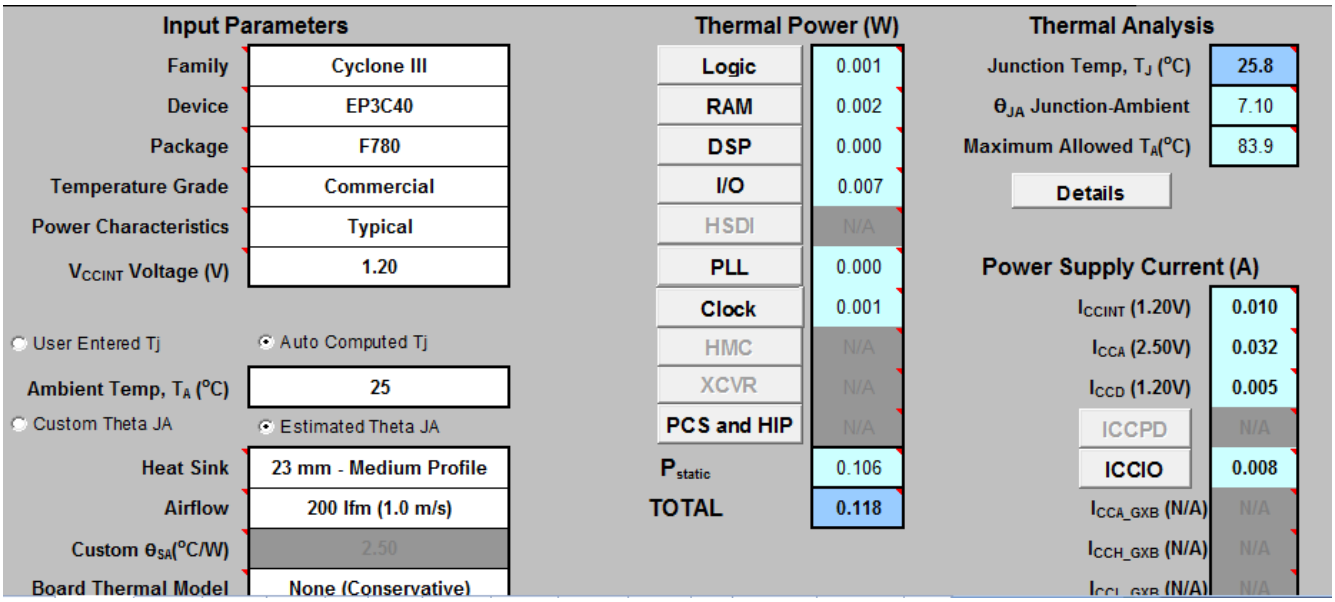

Figure 19. Estimating power of BPSK.

very good performance. Also, if designed QPSK modulator in this paper was compared to previous works, it could be obtained to advantages.

REFERENCES

Das A (2010). Digital Communication: Principles and System Modelling. Springer-Verlag Berlin Heidelberg.

Elamary G, Chester G, Neasham J (2009). A Simple Digital VHDL QPSK Modulator Designed Using CPLD/FPGAs for Biomedical Devices Application. Proc. World Congress Eng. 1:376-381.

Morrow R (2004). Wireless Network Coexistence. McGraw-Hill Professional Press, New York.

Popescu SO, Gontean AS (2011). Performance comparison of the BPSK and QPSK modulation techniques on FPGA. Proceedings of the 17th International Symposium for Design and Technology of Electronics Packages, Timisoara, Romania pp. 257-260.

Popescu SO, Gontean AS, Ianchis D (2011). Implementation of a QPSK system on FPGA. Proceedings of the 9th IEEE International Symposium on Intelligence Systems and Informatics, Subotica, Serbia pp. 365-370.

Sharma S, Kulkarn S, Pujari V, Vanitha M, Lakshminarsimhan P (2010). FPGA Implementation of M-PSK Modulators for Satellite Communication. Adv. Recent Technol. Comm. Comput. (ARTCom) pp. 136-139

Song W, Yao Q (2010). Design and Implement of QPSK Modem Based on FPGA. ICCSIT 2010 pp. 599-601.

Tianjun L, Wenrui D (2008). Typical Channel Coding and Modulation Scheme for Satellite Communication Systems. Antennas, Propagation and EM Theory, ISAPE 2008 pp. 1427-1430.

Xiong F (2000). Digital Modulation Techniques. *Artech House*. UK.