Scientific Research and Essay Vol.4 (11), pp. 1292-1301, November, 2009
Available online at http://www.academicjournals.org/SRE
ISSN 1992-2248 © 2009 Academic Journals

Full Length Research Paper

FPGA based digital electronics education and a simulator core design for a/d communication

Vedat Kiray* and Azamat Jambulov

International Ataturk Alatoo University, Industrial Electronics Department, Bishkek, Kyrgyzstan.

Accepted 23 September, 2009

In this study we present a Field Programmable Gate Array (FPGA) core (mega-function) design prepared to simulate the communication between an Analog to Digital Converter (ADC) and FPGA which were both located on an education board. The simulator core imitates ADS7824 coded ADC Integrated Circuit (IC). It is tested that the simulator core helps students to understand ADC theory better and make more practical and reliable designs related to ADC. We have preferred Graphics design for Educational purposes and all design steps were given in the study. This study included to a project called "FPGA based digital Electronic education" as an instructive and attractive example. This core can be used not only by students for educational purposes but also by Electronic Designers for general design purposes.

Key words: FPGA, ADC, simulator core.

INTRODUCTION

This study is a part of the project "FPGA Based Digital Electronic Education" presented at IKECCO`2006 in Bishkek (Kıray, 2006). The stages and details of the project were given at the conference.

There are lots of programs at the Universities in all over the world using the FPGAs as Education material. The names of the some similar studies were given at references part (Andreas and Ulrich (1993), Li and Chu, (1996), Mark (2004), Mark and Scott (2003), Camilo et al. (2005), Jerry, (2004). What makes our project different from others is that it aims to teach digital electronics and it involves some special design samples.

In this study, we are presenting an ADC simulator core design developed to overcome some difficulties encountered during communication applications between an ADC- integrated circuits (IC) and FPGA.

We observed that students studying on the FPGA education boards had some difficulties and were wasting time while designing circuits that had to communicate with ADC located on the same board. An increase on unsuccesful applications were causing delay on course plans and affecting negatively the students' performances. In order to overcome this problems, the simulator core was designed which simulates functions of ADC-Integrated circuit (ADS7824) located on FPGA board used at our laboratory. The design was prepared as an example and included in to the chapter of instructive and attractive examples in the FPGA based Digital Electronic Course Plan.

We have preferred Graphics design for Educational purposes. Pre-design studies are introduced below, then all Modules of the core are introduced separately in details and in the conclusion part, waveform simulation reports from the test example and advantages of the simulator core are assessed in terms of practicality, time saving and reliability.

ADC-IC-ADS7824

The ADS7824 is a low-power 12-bit sampling A/D converter with a four channel input multiplexer, S/H, clock, reference and a parallel or serial microprocessor interface. It can be configured in a continuous conversion mode to sequentially digitize all four channels. ADS7824 ADC integrated circuit which is placed at the FPGA board can be seen in Figure 1a and its schematic representtation can be seen in Figure 1b. Functions of ADS7824 are imitated according to its timing waveforms at simulator core design. Except analogue inputs, all input and output pins of the ADS7824 are located on simulator core.

*Corresponding author. E -mail: vkiray@iaau.edu.kg. Tel: +996 312 631425. Fax: +996 312 631432.

Figure 1a. ADS7824 ADC IC.

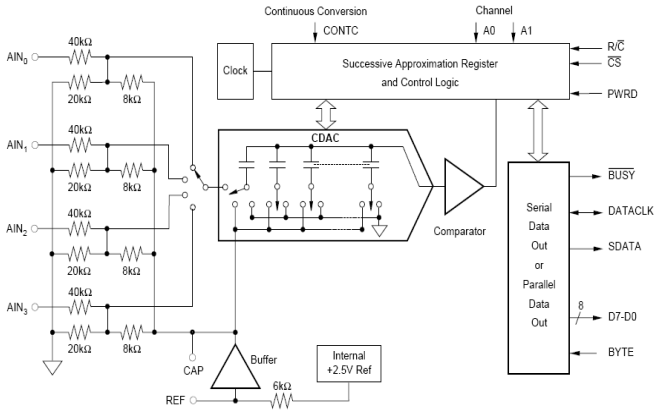

Figure 1b. ADS7824 hardware architecture.

PRE-DESIGN STUDIES

We have divided the design into four steps in order to make it understandable and instructive. The first step was named as pre-design study and the interactive signals were created without taking the regular modules into consideration. The aim of the first step is to prepare necessary small devices to generate the signals which are shown in the Figures 2 - 3 and understand the relationship among them. That's why all signals are shown as outputs in the Figures 2 and 3. Signal relations and timing of signals such as R\C, CS, BUSY, BYTE, DATABUS and SDATA are arranged according to ADS7824 datasheet. There are differences between the serial and parallel conversions. Although signal names are the same, different devices are needed to generating the signals.

The signal and timing pre-simulation results for serial and parallel conversions and consistency of signals between the datasheets and pre-simulation results can be seen in Figure 2 and 3. The general signal and timing properties are arranged in Table 1.

ADC-SIMULATOR CORE DESIGN

Modules for data channel selection, parallel and serial conversions are developed at the rest three steps. All the modules seen in Figure A-1 at appendix are combined under a block named ADC_IC_SIM_1 seen in Figure 4. It is impossible to represent the analogue data at simulator. That's why the 4 different 12-bit extra data inputs named TEST_DATA _IN_A, B, C and D were used instead of analogue data. The rest inputs and outputs are the same with ADS7824 IC. After testing any design by using the ACD simulator core, the inputs and outputs connected to the simulator core will be connected to those pins devoted to ADS7824 in the FPGA.

Data channel selection module

This module simulates the ADS7824 data channel selection function. Figure A-2 at appendix shows internal design of data channel selection module. The module consists of four 12-bits Dff registers, a multiplexer and a decoder. All channel outputs located after 12-bits registers are connected to multiplexer. Decoder and the multiplexer work parallel. While decoder makes the output of selected channel active, the multiplexer sends the selected data of the channel to out of the module. Both of them complete their functions according to position of CHN (3.0).

A parallel conversion module

All data can be received as serial or parallel after the completion of analog to digital conversion in ADS7824 IC. According to simulator's PAR-SER pin position (0 or 1); the parallel or serial conversion module is selected. 12-bit parallel data in 8-bit channel is sent in two stages: firstly 11-4 bits of data are sent and then the rest 3-0 bits are sent. The design of the module can be seen in Figure A-3. Main function of this module is to imitate the operation of 12-bits parallel data getting through 8-bits bus in two stages. BYTE signal plays active role for this operation. The first byte (11-4 bits) is received while BYTE signal is low and then second byte (3-0) is received while BYTE signal is high. There is an assistant module named schaltung3 used to generate BUSY_PAR signal. Main function of the assistant module is to make delay.

Serial conversion module

The operation of this module is based on shift register and counter logics. Serial data reading starts with CS or RC signal. There are three assistant blocks. First one is

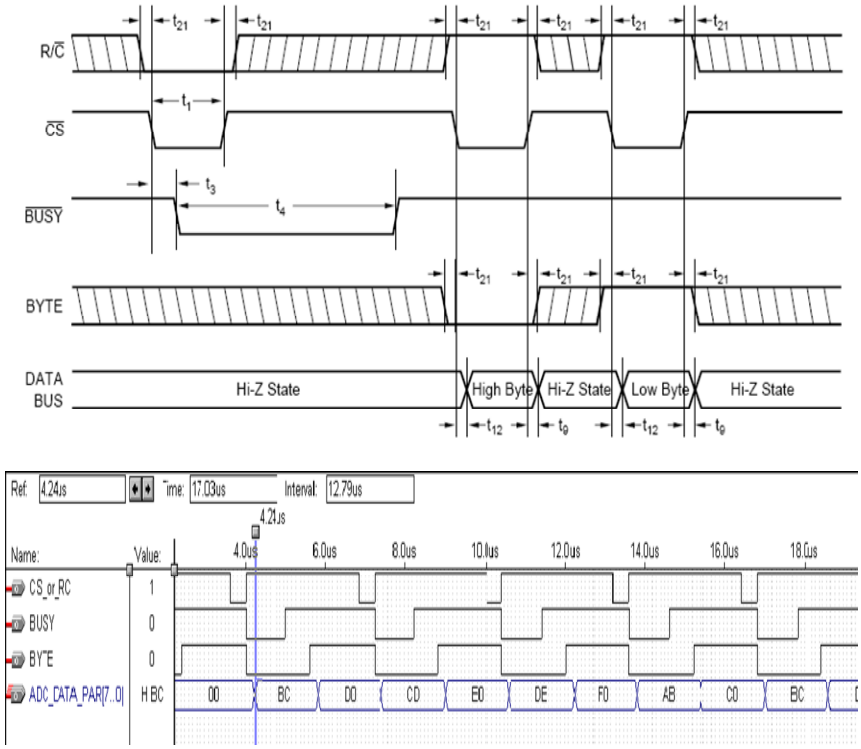

Figure 2. Signals in parallel conversions.

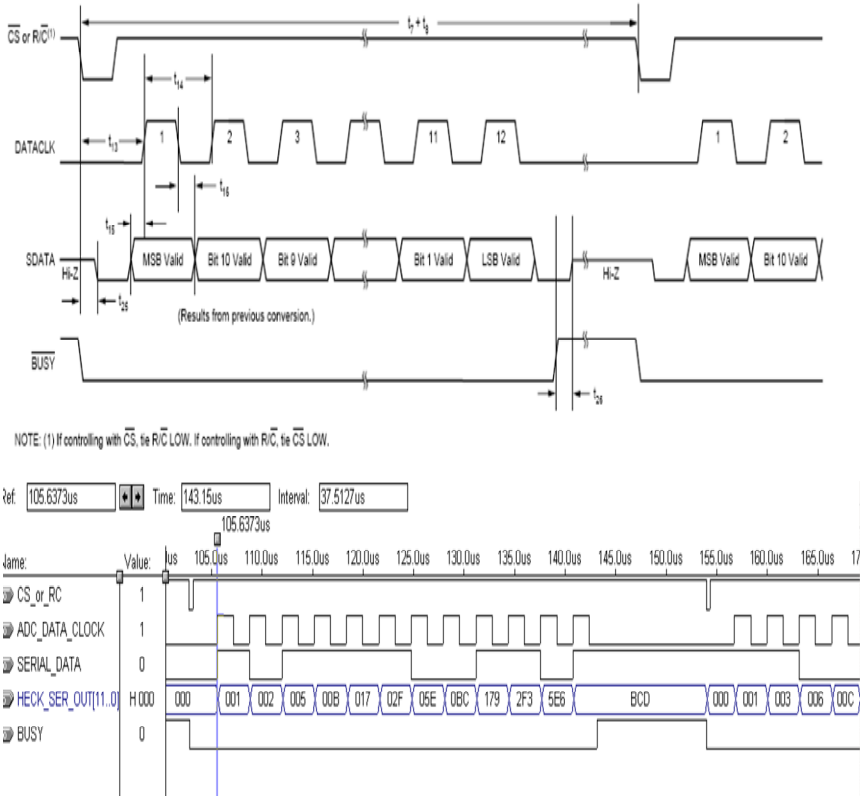

Figure 3. Signals in serial conversions.

Table 1. ADS7824 signal and timing properties.

SYMBOL	DESCRIPTION	HIN	TYP	MAX	JNITS
t_1	Convert Pulse Width	0.04		12	us
t_2	Start of Conversion to New Data Valid		15	21	us
t_3	Start of Conversion to BUSY LOW			S5	ns
t_4	BUSY **LOW**		15	21	us
t_5	End of Conversion to BUSY HIGH		90		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		15	21	us
t_8	Acquisition Time		3	5	us
$t_7 + t_8$	Throughput Time			25	us
t_9	Bus Relinquish Time	10		83	ns
t_{10}	Data Valid to BUSY HIGH	20	60		ns
t_{11}	Start of Conversion to Previous Data Not Valid	12	15		us
t_{12}	Bus Access Time and BYTE Delay			83	ns
t_{13}	Start of Conversion to DATACLK Delay		1.4		us
t_{14}	DATACLK Period		1.1		us
t_{15}	Data Valid to DATACLK HIGH	20	75		ns
t_{16}	DATACLK LOW to Data Not Valid	400	600		ns
t_{17}	External DATACLK Period	100			ns
t_{18}	External DATACLK HIGH	50			ns
t_{19}	External DATACLK LOW	40			ns
t_{20}	CS LOW and R/C HIGH to External DATACLK HIGH (Enable Clock)	25			ns
t_{21}	R/C to CS Setup Time	10			ns
t_{22}	CS HIGH or R/C LOW to External DATACLK HIGH (Disable Clock*	25			ns
t_{23}	DATACLK HIGH to SYNC HIGH	15		35	ns
t_{24}	DATACLK HIGH la Valid Data	25		55	ns
t_{25}	Start of Conversion to SDATA Active			83	ns
t_{26}	End of Conversion to SDATA Tri-Siate			83	ns
t_{27}	CS LOW and R/C HIGH to SDATA Active			83	ns
t_{28}	CS HIGH or R/C LOW to SDATA Tri-State			83	ns
t_{29}	BUSY HIGH to Address Valid			20	ns
t_{30}	Address Valid to BUSY LOW	500			ns

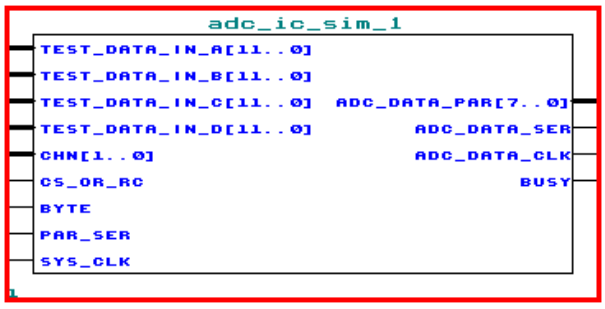

Figure 4. ADC-simulator block diagram.

"edge detect" block. It detects the falling edge of the CS or RC signal. Second one is "on_off_pulse" block. Its function is to provide necessary pulse for serial data reading. SYS_CLOCK pulse is 64 times slower than SYS_CLK pulse. At real applications, 12 bits serial data reading must be completed in 25 µsn according to datasheets of ADS7824. The third assistant block, schaltung3, is used for a delay. After making write signal high, firstly shaltung3 output will be high too, but after a while its output will be low again. The delay time can be arranged by using SYS_CLOCK2 signal. The comparator, at the output of the counter, controls the number of pulses. After the 12th pulse, the system is made passive by using the "e equal b" signal of comparator. New serial data reading starts with the new CS or RC. The Serial Conversion module architecture can be seen in Figure A-4 at the appendix.

Busy signals

At the end of the parallel or serial conversion, simulator

core must send a BUSY signal to circuit which will be connected to the simulator core. Each conversion spends different amount of time and they need different busy signals, so at the end of the conversions related proper busy signal is sent by using multiplexer (Figure. A-1 for block diagram).

Conclusion

Altera Quartus II program is used to test the simulator core. An example was developed to test performance of the simulator. ABC, BCD, CDE and DEF values were given from the test inputs and serial-parallel outputs were observed by changing channel selection bits. All simulation results for the simulator core can be seen in Figure A-5a and A-5b at appendix. After completing the general simulation studies, Inputs and outputs which were connected to the simulator core, this time will be connected to those pins devoted to ADS7824 in the FPGA for hardware tests.

This study is important for two reasons:

a) A general example for students, which explains all steps of the design in details.
b) A good similator toll for designers, which makes any ADC related design easy.

At the studies of simulation, if you use the simulator core, you will save time and it will be more practical and reliable. It is a reality that for professional studies HDL is better than schematics design, but especially for educational purposes this simulator core was designed by using Graphic editor.

FPGA based Digital Electronics Education was started as a project at International Ataturk Alatoo University in corparation with Zurich Technology University in 2006.

After teaching how to use the basic componets and some first level examples, some instructive and attractive projects were developed for the FPGA based Digital Electronic Education program. The Similator core design is one of them. The other four instructive and attractive projects are “clock-calender”, “calculator” ,“basic CPU” and “PID controller” designs. These projects will also be presented.

REFERENCES

Andreas K, Ulrich G (1993). FPGA Applications in Education and Research Proc. 4th EUROCHIP Workshop, Toledo, pp. 260-265.
Camilo QM, Dolores V, Mª Jose M, Luis F-F, Enrique M (2005). Digital Electronics Learning System Based on FPGA Applications, 35th ASEE/IEEE Frontiers in Education Conference.
Jerry K (2004). ALDEC, Inc. The Challenges of Modern FPGA Design Verification FPGA and Structural ASIC J.
Kıray V (2006). FPGA based Digital Electronic Education, IKECCO 2006, Bishkek, pp. 104-110.
Li Y, Chu W (1996). Using FPGA for Computer Architecture/Organization Education, IEEE Computer Society Technical Committee on Computer Architecture Newsletter, IEEE Computer Society Press. pp. 31-35.
Mark H (2004). An Fpga-Based Digital Logic Lab For Computer Organization And Architecture, J. Comp. Sci. Coll. 19(5): 214-227.
Mark H, James H, Scott H (2003). Harnessing FPGAs for Computer Architecture Education, Proceedings of the 2003 IEEE International Conference on Microelectronic Systems Education (MSE’03).

APPENDIX

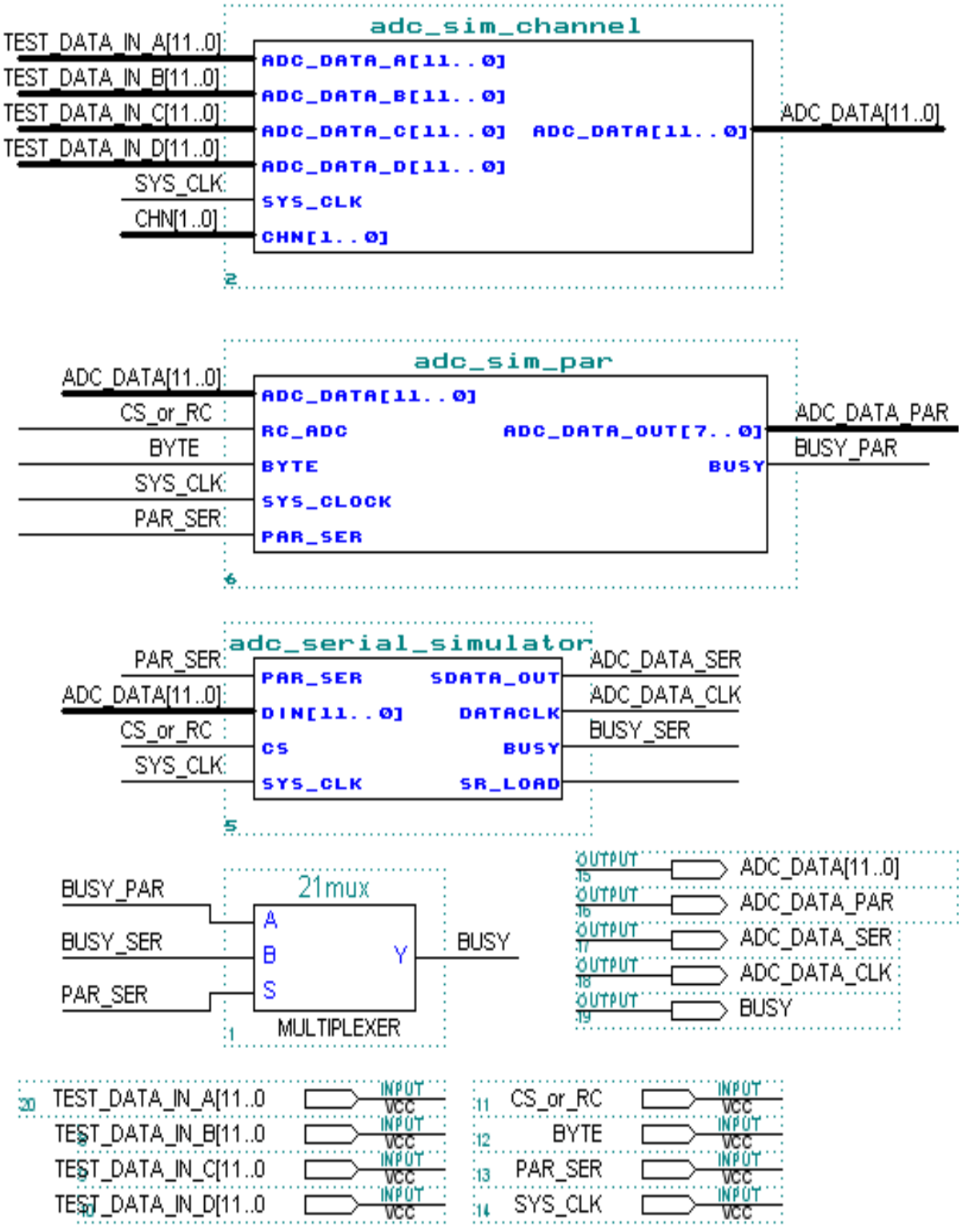

Figure A-1. ADC-Simulation Modules.

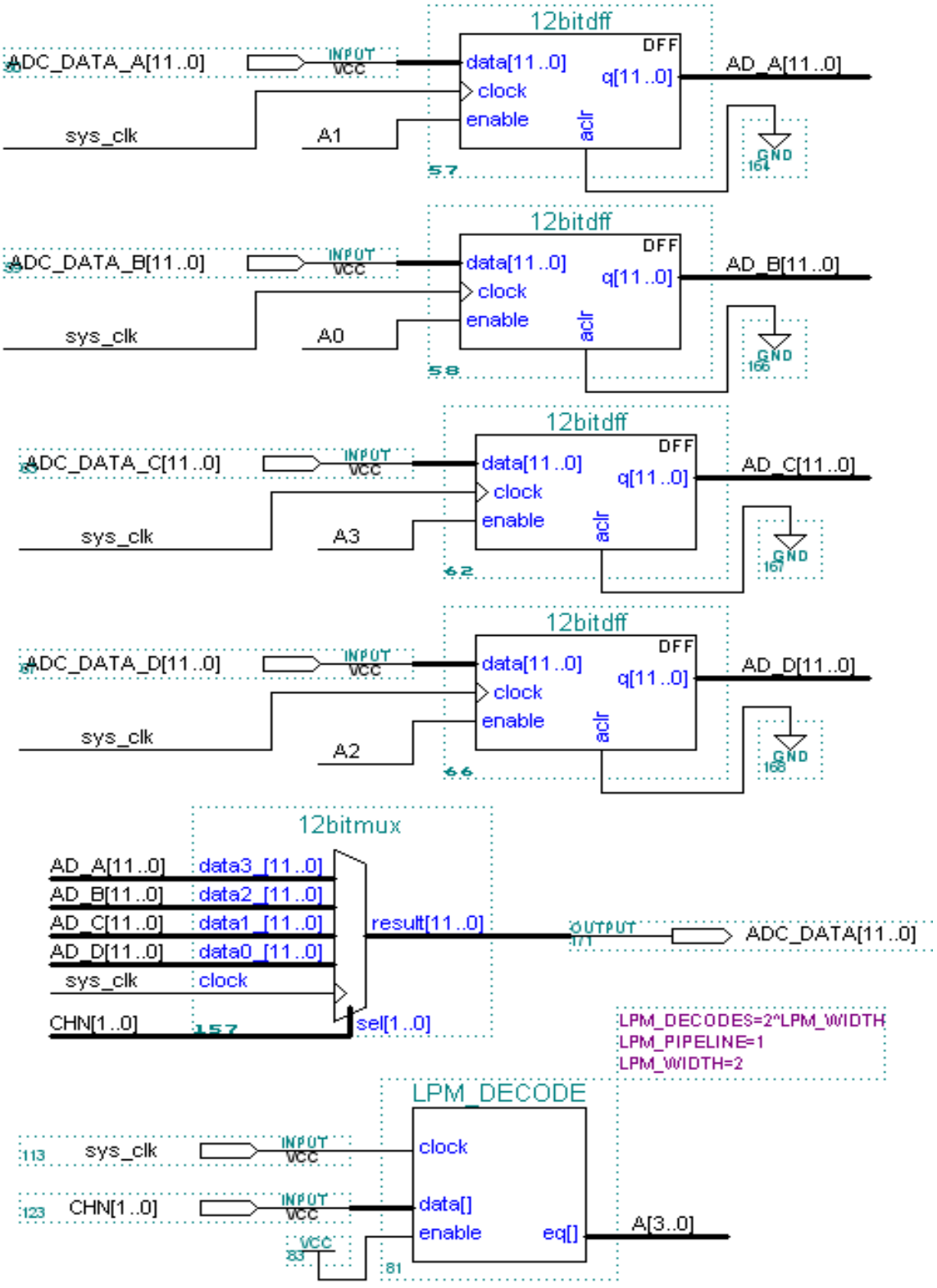

Figure A-2. ADC-Simulator channel select module.

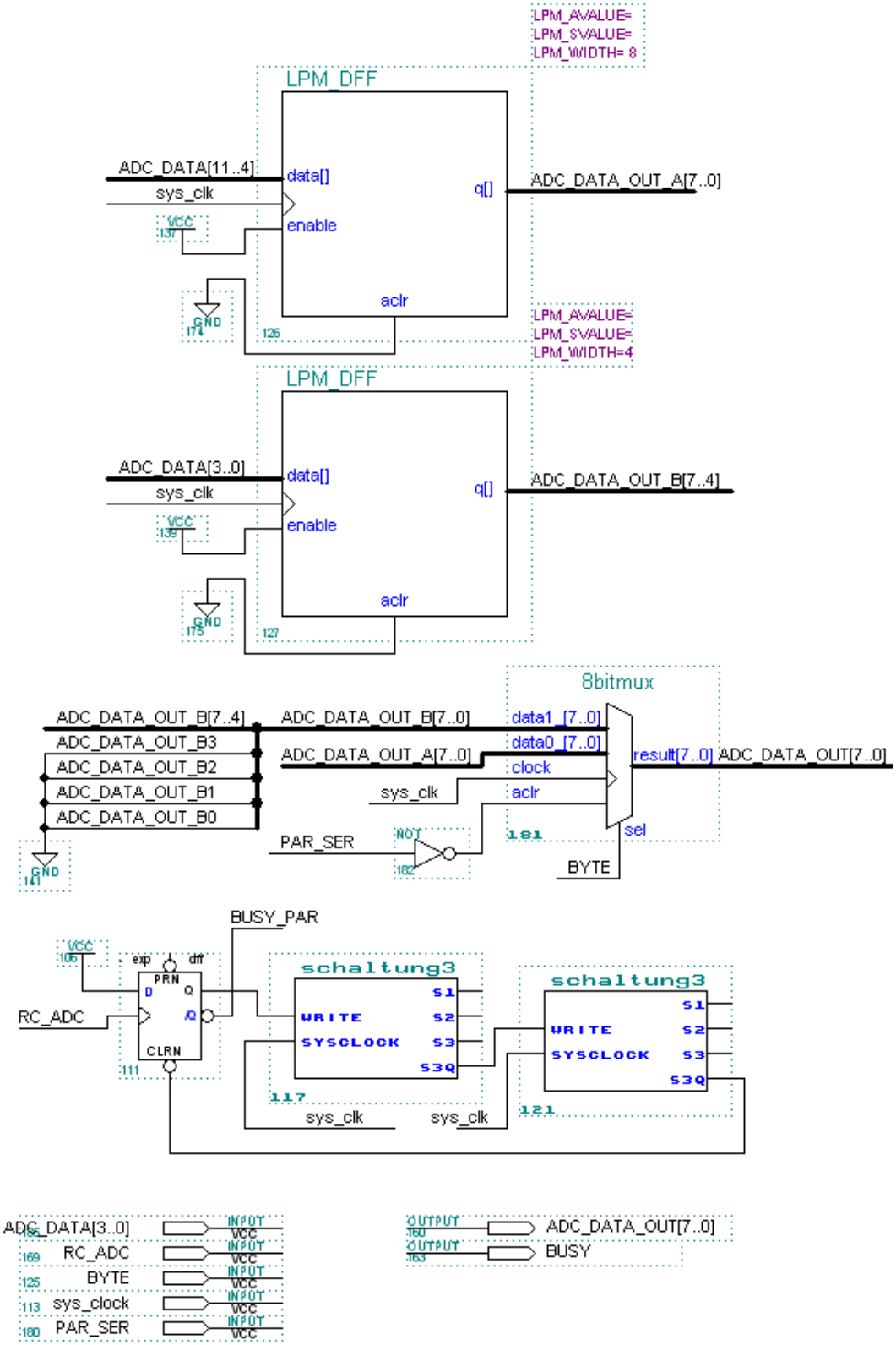

Figure A-3. ADC- Simulator parallel conversion module.

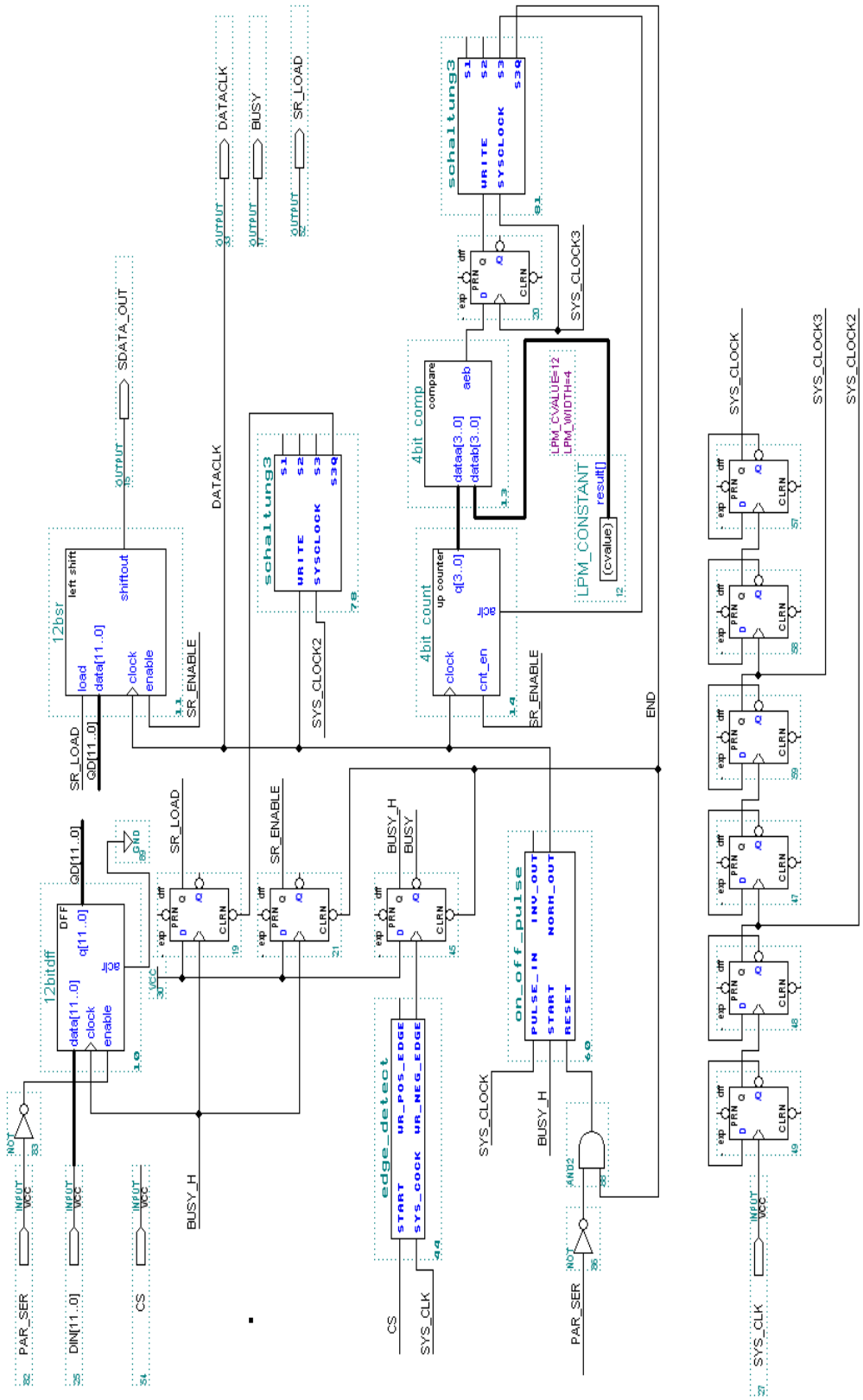

Figure A-4. ADC0 Simulator serial conversion module.

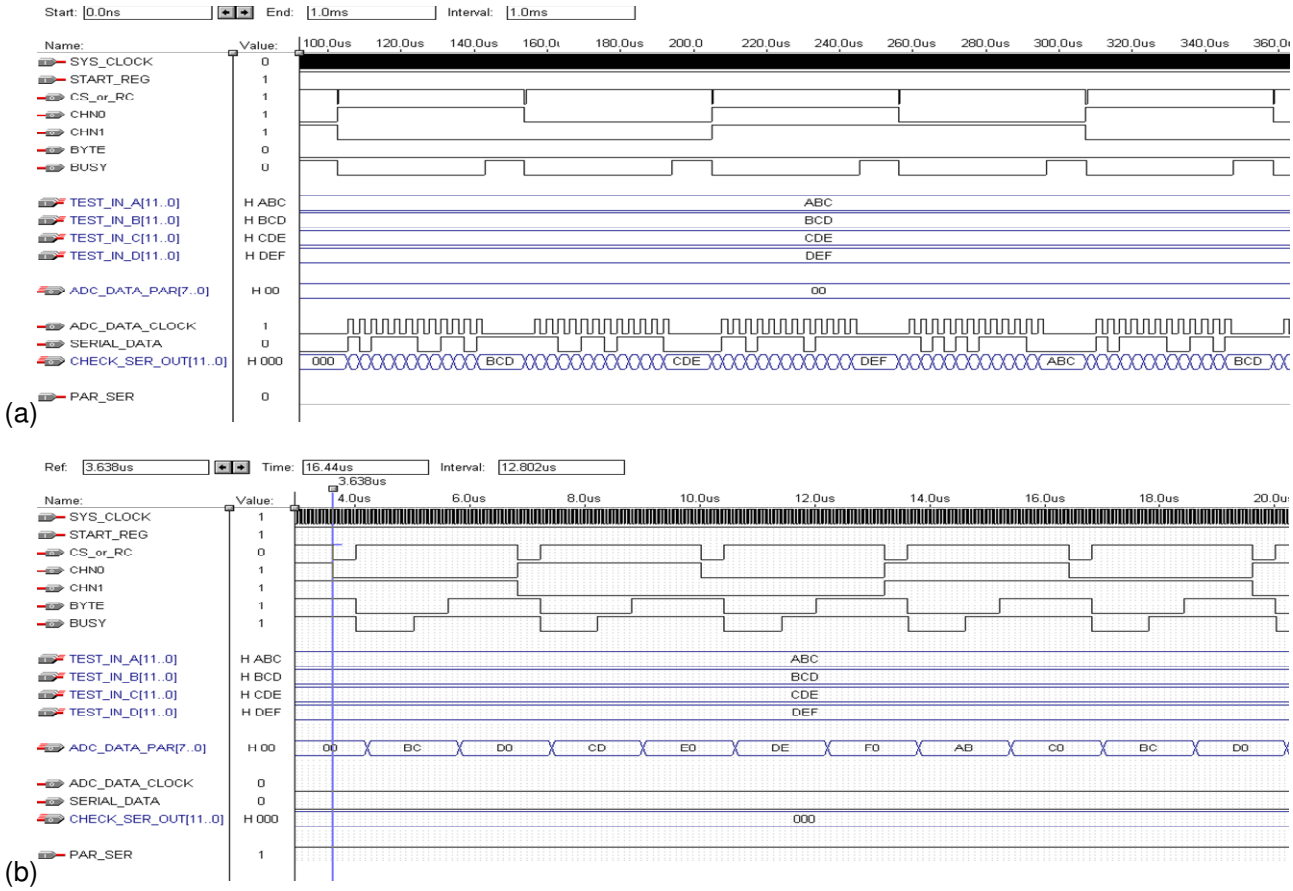

Figure A-5. ADC-waveform simulation reports. a: Serial reading b: parallel reading.